A low power and high gain CMOS LNA for UWB applications using a gate inductor

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Abstract

A new ultra wideband low noise amplifier is presented. The ultra wideband LNA consists of two simple amplifiers. A common source topology by gate inductor is adopted for input stage to achieve wideband input matching and wider bandwidth. The second stage by noise cancelling technique achieves high flat gain. Realized in standard TSMC0.18μM CMOS. It achieves a maximum power gain of 11.8 dB, a bandwidth of 10GHz and 4.9dB minimum noise figure. The power consumption is 22mW from a 1.8V supply.

Keywords: UWB, CMOS, gain-flatness, Noise figure, low noise amplifier.

Introduction:

In recent years, the Federal Communications Commission (FCC) in the US approved the use of ultra-wideband technology for commercial applications in the 3.1-10.6 GHz. UWB performs for high-speed uses such as wireless personal area networks, medical-imaging systems, ground and vehicular penetrating radars and high-speed indoor networking[1-6].

LNA as the first module of UWB receiver has important influence on the sensitivity and dynamic range of the whole receiver system. LNA needs to features such as broadband input matching to minimize the return loss, sufficient gain to suppress the noise of a mixer, low noise figure to enhance the sensitivity of a receiver, small die area to reduce the cost and low power consumption[2-7]. In addition, the LNA input impedance should be close to 50Ω across the band from 3 to 10 GHz.

Many topologies have been presented in LNA designs, such as cascade amplifiers, distributed amplifiers, current-reused amplifiers and feedback amplifiers. The distributed amplifier provides good linearity and sufficient matching conditions and improve gains at higher frequencies. The resistive feedback has
advantage such as gain flatness, noise figure and matching and it tends to degrade the noise performance because of the feedback resistor peak near the input stage.

This paper introduces a gate inductor to achieve high and flat gain and wider bandwidth. The gain $S_{21}$ is approximately equal to 11 dB and the minimum NF is below 5 dB in the entire band.

The paper is organized as follows. Section 2 shows proposed UWB LNA. Section 3 analyzes the proposed LNA and section 4 gives the simulation results and compares its performance with recently reported CMOS LNAs.

**CIRCUIT DESIGN OF UWB LNA:**

The schematic of the UWB LNA is shown in Fig. 1. In the proposed UWB LNA, a resistive feedback and gate inductor are adopted in the first stage for bandwidth enhancement and input impedance matching, while a noise cancelling technique is adopted in the second stage for high gain.

![Fig.1. The proposed UWB LNA](image)

**ANALYSIS OF PROPOSED UWB LNA:**

The small signal equivalent circuit of the first stage is illustrated in Fig. 2. The circuit of the proposed UWB LNA is shown in Fig. 1, which is composed of two simple amplifiers. The main problem with the use of resistive in LNA is that the parasitic capacitances due to the miller effect, and hence lead to degradation in input impedance at high frequency.
For input matching, the LC network combined with the Lg and the intrinsic capacitances to form a LC ladder network for achieving a wideband matching. Assuming that the input miller effect is relatively small.

\[ Z_1 = \frac{1}{j\omega C_{gs1}} \]  
\[ Z_2 = j\omega L_g + \frac{1}{j\omega C_{gs2}} \]  
\[ Z_{in} = \frac{Z_1Z_2}{Z_1Z_2 - \left(\frac{g_m_1r_{o1}r_{o2}}{j\omega C_{gs1}Z_2} - \frac{g_m_2r_{o1}r_{o2}}{j\omega C_{gs2}Z_2}\right)} \]  

Fig. 2 gate inductive topology and equivalent model
As can be seen in the equivalent ac model, the Lg inductor split the parasitic capacitance (C_{gs} and C_{gd}) at the input of amplifier and facilitates bandwidth extension.
Input impedance of the proposed LNA can be expressed as

Fig. 3 illustrates the effect Lg on the input impedance.
Fig. 3 illustrates the effect $L_g$ on the S11. The gate inductor is connected in series to parasitic capacitance and forms LC network. where $\omega_0 = \frac{1}{\sqrt{L_g C_{gs}}}$ and $Q_0 = \frac{\omega_0 L_g}{R_{Lg}}$.

When $\omega$ is lower than $\omega_0$, the signal at $M_1'$s gate is amplified. Therefore, a wider bandwidth and flat gain is available.

When $\omega_0$ is near to lower than $\omega_p$, an overpeaking of gain will occur and it may lead to stability issue. On the other side when $\omega_0$ is higher than $\omega_p$, the LNA cannot get effective gain. $M_3$ and $M_4$ are used to combine the signal and subtract the noise of $M_1$. By adding $M_3$ the part of current of $M_3$ flows into $M_1$, which increases $g_{m1}$. The amplifier $AX$ is implemented in a common-source configuration by $M_4$ and $AY$ is implemented in a common-gate configuration by $M_3$. $AX$ and $AY$ are expressed as[11].

\[
A_X = g_{m4} R_{L2} \\
A_Y = \frac{V_{D3}}{V_{D2}} = \frac{R_1 r_{o4} A_L}{R_2} \frac{1 - r_{o1}^2}{g_{m3} g_{m2} (1 + r_{o2}^2)} \\
R_b = \frac{R_2}{1 + g_{m4} (r_{o4} R_1 r_{o2})} \\
R_{L2} = R_3 \parallel r_{o4} \parallel (g_{m3} r_{o3} R_{L1}) \parallel R_b
\]
The main noise source in this LNA are the channel noises of M1 and M2 and the thermal noise of the feedback resistor RF.

**Fig.4. effect Lg on the S21**

**Fig.5. model transistors thermal noise**
Modeling the channel thermal noise of $M_1$ by a current source between drain and source $I_{n,M1}$ is defined as
\[ \overline{I_{n,M1}^2} = 4KT \overline{I_n}^2 g_{m1} \]  
(8)

$\overline{I_n}$ is a noise parameter and $\alpha = g_m/g_{do}$, where $g_{do}$ is the channel conductance for $V_{DS}=0$.

The noise factor $F$ can be derived by
\[ F = \frac{\overline{V_{n,1}^2}}{\overline{I_{n,1}^2}} = \frac{4kT\overline{I_n} g_{m1}^2}{4kT\overline{I_n} g_{m,NC}^2 + 4kT R_L g} \]  
(9)

\[ \overline{V_{n,1}^2} = \frac{4kT \overline{I_n} g_{m1}^2}{g_{M1}^2} + 4kT R_L g \]  
(10)

\[ \overline{I_{n,1}^2} = \frac{4kT \overline{I_n} g_{m1}^2}{g_{M1}^2} \omega^2 C_{g1}^2 + \frac{4kT R_L g^2}{g_{M1}^2} \omega^2 C_{g1}^2 \]  
(11)

Fig.6 illustrates the effect $L_g$ on the noise figure.

**SIMULATION RESULT :**

Fig.7 shows the simulated results of input reflection coefficient ($S_{11}$). The simulated $S_{11}$ is lower than -10 dB over the entire 3.1-10.6 GHz. The simulated results of output reflection coefficients ($S_{22}$) is shown in Fig.8. The $S_{22}$ is less than -10 dB. Fig.9 shows the simulated gain. The maximum $S_{21}$ is 11.8 dB. Fig.10 indicates the simulated reverse isolation ($S_{12}$) for the UWB LNA circuit. An $S_{12}$ is less than -35 dB. The simulated NF is shown in Fig.11 and minimum NF is 4.9 dB. The proposed circuit consumes 22 mW from 1.8 V supply voltage. The component values of our proposed circuit are also shown in Table.1. Table 2
summarizes the performance of the LNA and compares with the other reported circuit performance. The proposed circuit shows a good performance with low power, high gain and low noise.

Fig.7. simulated S11

Fig.8. simulated S22

Fig.9. simulated S21

Fig.10. simulated S12
**TABLE 1 - Component values of the LNA**

<table>
<thead>
<tr>
<th>Transistor size</th>
<th>(W/L)_1</th>
<th>(W/L)_2</th>
<th>(W/L)_3</th>
<th>(W/L)_4</th>
<th>(W/L)_5</th>
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<tr>
<td></td>
<td>260/0.18</td>
<td>110/0.18</td>
<td>36/0.18</td>
<td>80/0.18</td>
<td>60/0.18</td>
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<table>
<thead>
<tr>
<th>Inductor value</th>
<th>L_3</th>
<th>L_2</th>
<th>L_1</th>
<th>L_2</th>
<th>L_3</th>
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<tr>
<td></td>
<td>5.3nH</td>
<td>0.7nH</td>
<td>6.1nH</td>
<td>6.5nH</td>
<td>1.9nH</td>
</tr>
</tbody>
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<table>
<thead>
<tr>
<th>Resistor value</th>
<th>R_F</th>
<th>R_1</th>
<th>R_2</th>
<th>R_3</th>
<th></th>
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<tbody>
<tr>
<td></td>
<td>200Ω</td>
<td>75Ω</td>
<td>56Ω</td>
<td>1.5kΩ</td>
<td>-</td>
</tr>
</tbody>
</table>

**TABLE 2 - Performance of the proposed UWB LNA and comparison with other UWB LNAs**
References:


