A 0.8-V 712-nW delta–sigma modulator for low-power biomedical application

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Abstract

This paper presents the design of a low voltage and low power delta-sigma modulator as a sensing stage for biomedical application. This delta-sigma modulator designed for portable electronic system in digitalizing biomedical signals such as pacemaker which detects and assists the heart’s natural electrical activity. The delta-sigma architecture is implemented as third-order distributed feed forward delta-sigma modulator. Additionally, the use of transistors in weak inversion region saved power. The designed modulator has consumes only 712nW for 250 Hz bandwidth. The dynamic range of this designed modulator is 53db. The core chip size is 1mm² by using the 0.18μm standard CMOS process.

Keywords: delta–sigma modulator, low-power biomedical application

Introduction:

The demand of low voltage, low power circuit for portable electronic systems such as wireless communication device, consume battery powered biomedical devices have increased recently [1]. In biomedical applications it is important to design low power, low voltage circuits, it can reduce the number of battery cells for low weight and small system size and can increase the operation time for biomedical application [2]. A biomedical device receives information regarding body’s signals [3]. The body signals are very low frequency therefor the flicker noise issue of devices for this application will be very important. Due to the increasing development of biomedical devices, they require a suitable analog to digital converter (ADC) that converted body analog signals to digital signals which can be processed by device, increases. Because of high dynamic range for low signal bandwidth with low power consumption, the delta sigma modulator is suitable for the sensing stage. In the third-order delta sigma modulator the effect of noise shaping is more than one-order and second-order delta sigma modulator and improvement signal to noise ratio (SNR), this modulator consists of three integrators, one-bit comparator and one-bit DAC for feedback loop, this single bit signals of comparator output converted into multi-bit signals at Nyquist sampling rate for biomedical application. By using oversampling and noise shaping technique can achieve high SNR in delta-sigma modulator.
In our design, implement third-order delta-sigma modulator as feed forward structure. For op amp’s integrators we use transistor in weak inversion region to maximize input device transconductance as minimized flicker noise. At the same time use of transistors in weak inversion region can minimized power consumption moreover power saving can achieve by using low oversampling ratio (OSR).

**Delta–sigma architecture**

Delta sigma modulator has proven to be very suitable for low frequency, high performance application. The designed modulator is a distribute feed forward structure of third-order delta-sigma modulator. The most significant factor is that there is an extra signal path from the input of the modulator to the quantizer in the feed forward architecture. And only the quantization noise element is processed in the loop filter for the modulator. This causes the Input signal to be completely removed in the loop filter path [4]. Between a switched capacitor (SC) and a conventional active RC for integrator, we choose SC circuit [5]. SC structure is preferred to active RC because it is easily simulated, compatible with VLSI CMOS, processed and insensitive to clock jitter [6].

![Fig.1 Distributed feed forward delta sigma modulator](image)

**Circuit implementation**

- **OTA**

The operation amplifier (op amp) in the integrator determines on the operation speed and performance of the modulator. The transistors have biased in weak inversion region. The Use of transistor in weak inversion region minimizes power consumption and maximized input transconductance. The Use of transistor in weak inversion region has a few disadvantages, the linearity of transistors in this region affects and worsens but for human body signal’s amplitude linearity is acceptable. Fig.2 shows the designed amplifier structure, which is the folded-cascade OTA.
The thermal noise and the flicker noise power of the OTA are calculated by using Hspice noise simulated. The dynamic range (DR) of the OTA is calculated by ratio between the input signal powers to the noise power, as shown below:

\[
DR = 10\log \frac{P_{\text{signal}}}{P_{\text{thermal}+\text{flicker}}}
\]  

(1)

To calculate the input signal power it is assumed that the maximum input amplitude is 0.4V according to body signals.

In discrete time (DT), the common mode feedback (CMFB) of an amplifier is a critical for low voltage and low power application because it sets the common mode output voltage to VDD/2 for maximum output swing and it also requires little power. Fig.3 shows the common mode feedback circuit. The advantage of this common mode feedback circuit is that the common mode feedback voltage is independent of transistor threshold voltage.

In the delta sigma modulator closer to the output stage the noise shaping effect is greater, so the others OTA have the same architecture with reduce current and performance to reduce power consumption.
Table.1 shows simulation results of the first OTA with an effective load capacitance of $C_{\text{Leff}}$. The OTA gain is 44.95db. The unity gain frequency is 81.08 kHz and the phase margin is 90°. The results indicate that the OTA provides satisfactory performance to the modulator.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>OTA</th>
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<tbody>
<tr>
<td>Supply voltage</td>
<td>0.8 V</td>
</tr>
<tr>
<td>DC gain</td>
<td>44.59 db</td>
</tr>
<tr>
<td>Phase margin</td>
<td>90°</td>
</tr>
<tr>
<td>Unity gain frequency</td>
<td>81.08 kHz</td>
</tr>
<tr>
<td>Power consumption</td>
<td>346.788 nW</td>
</tr>
<tr>
<td>Process</td>
<td>0.18 μm</td>
</tr>
</tbody>
</table>

Table.1 the first OTA performance

- Comparator

In the delta sigma modulator comparator is 1-bit ADC that quantizes in the loop filter and provides the digital output. In the third order delta sigma modulator, offset and hysteresis of two level quantizer are attenuated in the base band by noise shaping effect and can be filtered by decimation filter, so delta sigma modulator is insensitive to offset and hysteresis of the comparator. Fig.4 shows the regenerative latch with clock signal control [7]. Fig.5 shows the RS latch utilized to form a dynamic comparator. This comparator has some characteristic such as low power consumption and fast transition.
Fig.4 Regenerative latch

- Switched-capacitor modulator

Fig.6 shows the third order sigma delta modulator by feed forward architecture. The non-linearity of the feedback DAC may cause signal distortion because any non-ideality and non-linearity of DAC is compared to modulator input and less affected by noise shaping. For that reason, 1-bit DACs are typically used in sigma delta modulator. Moreover, 1-bit DAC is adapted to 1-bit comparator and reduces the modulator complexity.

Experimental results

Fig.7 shows the chip layout of the designed modulator by using the 0.18μm process. The core size is 1mm². The analog and the digital blocks are separated so that the sensitive analog blocks are not affected by digital noise.
Fig. 8 shows the simulated results of SNR. Non-idealities of the circuit are modeled at MATLAB/Simulink [8]. The OTA’s DC gain, unity gain band width are included is behavior model.

![Fig. 7 The chip layout](image1)

![Fig. 8 Simulated SNR](image2)

The parasitic capacitor at the input of OTA that causes settling of the input differential pair is not modeled. The power is measured as 876nw. the measurement results are minimized at table2.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>OTA</th>
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<tbody>
<tr>
<td>Supply voltage</td>
<td>0.8 V</td>
</tr>
<tr>
<td>Power consumption</td>
<td>712 nW</td>
</tr>
<tr>
<td>Peak SNR</td>
<td>30 dB</td>
</tr>
<tr>
<td>Dynamic range</td>
<td>49 dB</td>
</tr>
<tr>
<td>Sampling frequency</td>
<td>10 kHz</td>
</tr>
<tr>
<td>Signal bandwidth</td>
<td>250 Hz</td>
</tr>
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</table>
Table 2 Performance Summary

<table>
<thead>
<tr>
<th>Oversampling ratio</th>
<th>20</th>
</tr>
</thead>
<tbody>
<tr>
<td>Core size</td>
<td>1 mm$^2$</td>
</tr>
</tbody>
</table>

**Conclusion**

In this paper, a low power third order feed forward delta sigma modulator for use in biomedical system presented. This modulator operate at a supply voltage of 0.8 V. power consumption of the overall delta sigma modulator is 712 nw for the 250Hz band width. This modulator achieves SNR of 30db. It is suitable for different biomedical application.

**Reference**


