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Design and Functional Verification of 4 Bit Arbiter in Quantum Dot Cellular Automata

A. Rajesh [a], V.J. Arulkarthick [b], N. Rajeshwaran [c]

[a] *Research Scholar, Department of ECE, Shri Jagdhishprasath Jhabarmal Tibrewala University, Jhunjhunu Rajasthan, India.*
[b] *Professor, Department of ECE, JCT College of Engineering and Technology, Coimbatore, Tamilnadu, India.*
[c] *Professor, Department of EEE, Malla Reddy Engineering College, Hyderabad, Andrapradesh, India.*

Abstract

Reduction in the size of a device gains much attention nowadays. But the process of reducing the same gets more complicated. QCA is getting expedited to do the task. Because Quantum Dot Cellular Automata is dealing with the movement of electrons in a quantum cell, it is already like a partially done job. Various aspects of 2 and 3 input arbiters are discussed. A new 4 input arbiter design is introduced and verified by combining the QCA concepts which includes the basic elements Majority Gates and an inverter. This novel 4 Bit arbiter can be a fundamental block for multiple resources sharing networks with a reduced size and delay.

Keywords: Cellular Automata, Quantum Dot, Nanosize.

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Introduction

Quantum-dot Cellular Automata (QCA) is one among the important manifestations that are configured to be an effective substitute for CMOS technology for the approaching tomorrow. A crucial characteristic of this process, that dragged the eye of the numerous researchers is that it was depicted through its low energy consumption, high speed and smaller size in contrast to CMOS. The QCA is operating with two basic elements called Majority gate and Inverter. The fig 1 represents the QCA Cell of binary 1 and binary 0. The arrangement of cells in certain formats as shown in fig 2 leads to the formation of wire (used for the propagation), inverter and majority gate.

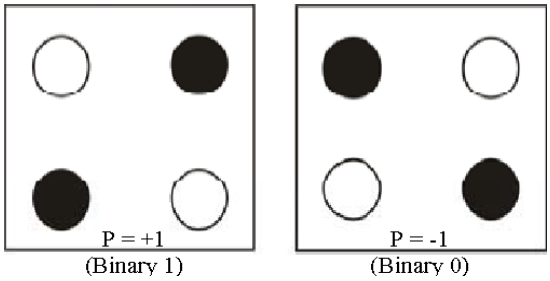

Figure 1: Binary 1 and Binary 0 Representation of Quantum Cells

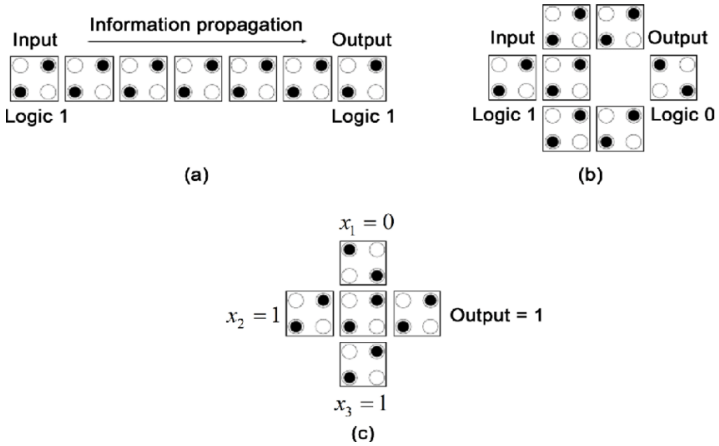

Figure 2: Wire, Inverter, Majority Gate

Arbiters are an indispensable part of the systems and are accustomed to sort out the contention issue at the place when several requests need to be managed for common resources. Moreover, with the constantly rising fashion in the reduction of size within the manufacturing procedure, Quantum-dot Cellular Automata (QCA) along with the characteristic of nanosize, power advantages may be a high-achieving factor in realizing upcoming Circuits. The Fundamental arbiter with two master and a slave is depicted below.

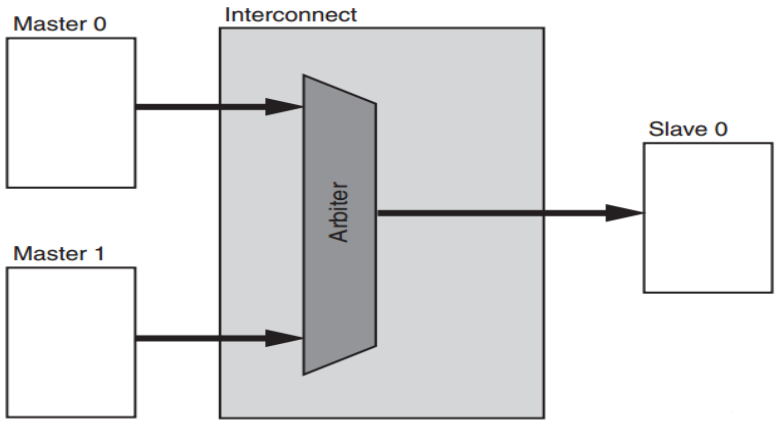

Figure 3: Arbiter

Arbiter

An Arbiter does a job similar to a cop of traffic at a crossroad who decides which vehicle can move first. With a single claim, an Arbiter swiftly approves the analogous activity; postpone the other requests unless the prioritized task is finalized. At the time of getting more than one request at the same time, the arbiter will choose the request to grant for primary access. General 4 input arbiter is given as follows.

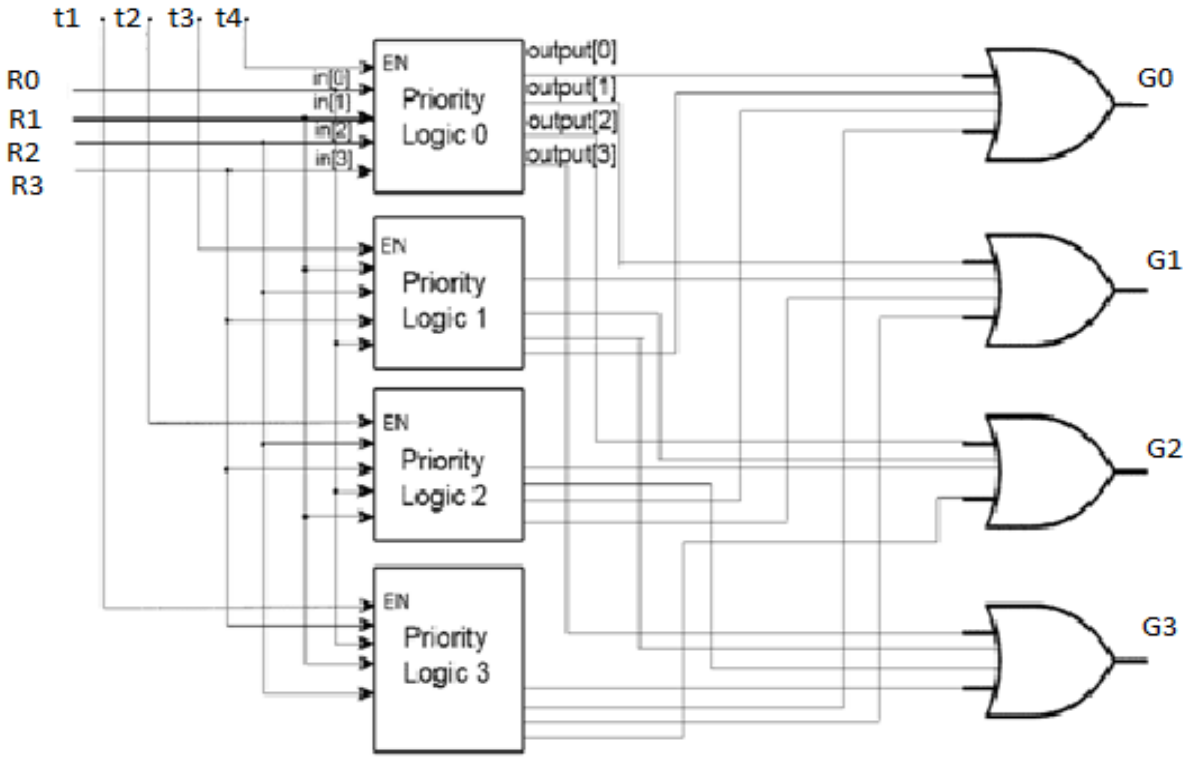

Figure 4: General 4 Bit Arbiter

Generally Priority logic works according to the priority assigned to each inputs. A typical Priority logic of 4 bit input obtained with the combinations of AND and OR gates is given as follows. In order to perform the AND and OR operation using Majority gate the any one input should be made to a constant value 0 and 1 respectively. Most of the gates such as NAND, OR, NOT, AND, XOR.XNOR can be achieved in QCA. Majority logic can be obtained with the cellular arrangements of Quantum cells and it is depicted symbolically as given in fig.

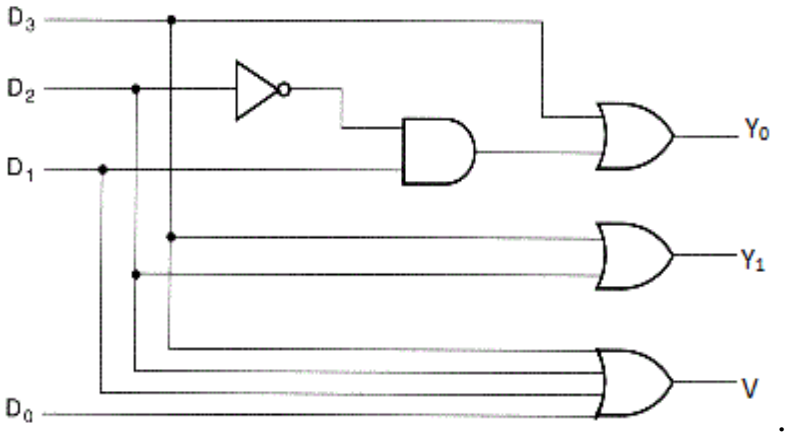

Figure 5: 4 Bit Priority Logic Diagram

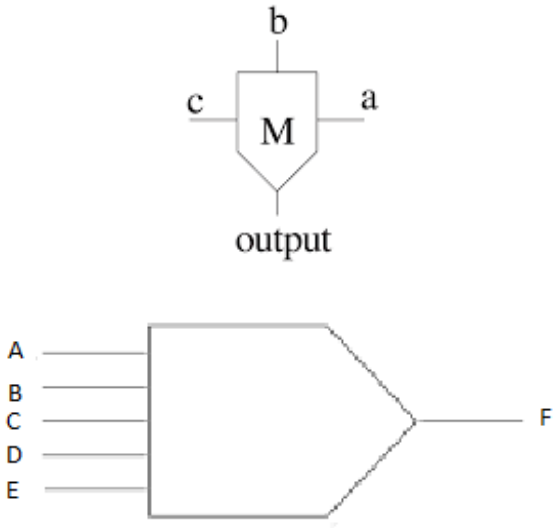

Figure 6: General 3 and 5 bit Majority Logic Symbol

Counter belongs to the category of Sequential circuits. This counters are used to count the pulses. The ring counter is designed in such a way that the output of the first block is fed to the input of the second block in a ring counter. The output of the final block is fed to the input of first block. The schematic of the ring counter and its implementation of ring counter using QCA is as follows.

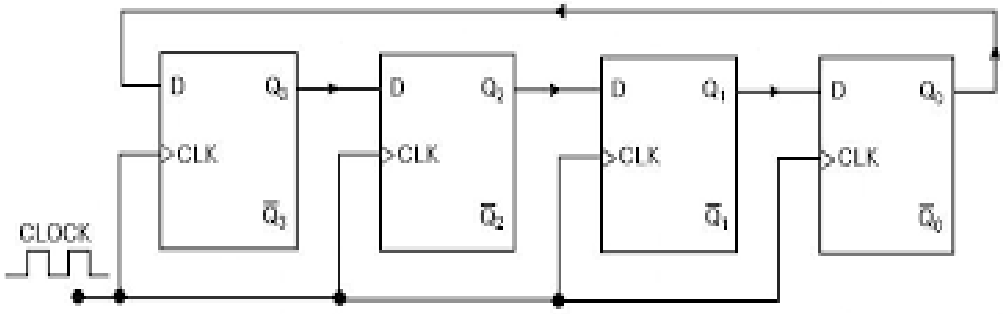

Figure 7: Schematics of Ring counter

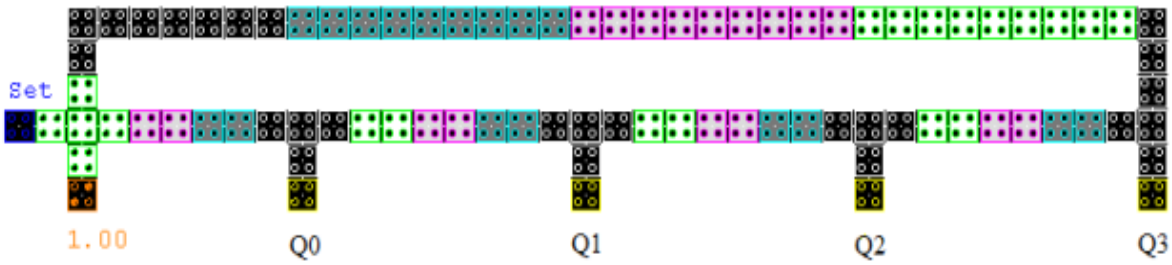

Figure 8: QCA Implementation of Ring counter

Waveform of Arbiter

The output waveforms is shown in figure 9. It consists of 4 request lines and 4 grant lines. The busy line is active if any one of the grant line is high.

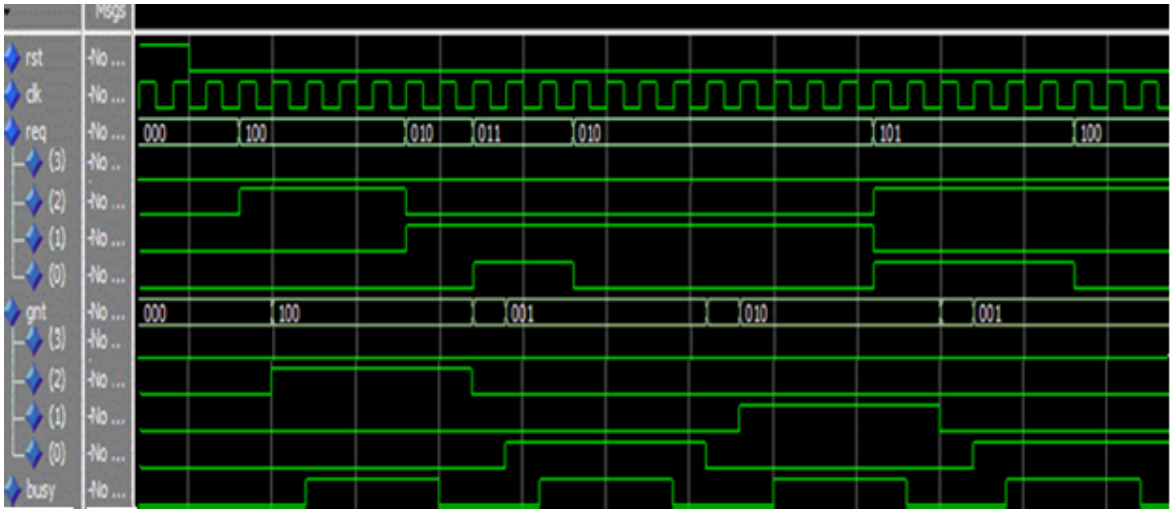

Figure 9: Waveform of 4 input arbiter

Conclusion

The conventional design of an arbiter will have a power consumption of 15.703 mW which is reduced to a 13.936 mW if the same design is implemented using the QCA cells. Also the cell area is reduced to 768 to 749square micron. The time improvement is 11.25% and reduction in area is reduced by 2.47%. The future work of this project deals with the replacement of conventional ring counter with a twisted ring counter which will further enhance the efficiency of arbiter.

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