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Design of Two New High-Performance Full Adders in Sub-threshold Region for Ultra-Low Power Applications

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Abstract

This paper presents two new structures of 1-bit full adder. It compares full adder sub-circuits and two proposed full adder circuits with common circuits in terms of propagation delay, power consumption, power delay product and square power delay product in sub-threshold voltage technology. HSPICE simulations show that all the proposed adders are improved significantly in power delay product and square power delay product parameters. The full adder structures are compared in 260 (mV) supply voltage.

Keywords: 1-bit adder, sub-threshold voltage technology, propagation delay, power consumption, high performance

Introduction:

Adders are usually the most common cells used in digital systems. For instance, these circuits may be applied in Arithmetic circuits and DSP systems. Power consumption and Delay time are two important parameters that must be decreased simultaneously. Power consumption is important more than Delay time, specially, for portable devices. Designing adder circuits in sub-threshold voltage is a suitable method for considerable reduction of power consumption [1]. In designing circuits at sub-threshold voltage, a source voltage should reduce gradually as much as the threshold voltage [1]. Consequently, a VLSI designer should use a kind of trade-off between Delay time and Power consumption. A comparison can be made with respect to circuits PDP (Power×Delay) to compensate for the parameters. In fact, this article aim at examining performance of these structures using supply voltage reduction. Of course, this paper defined P^2DP ($Power^2$×Delay) for making a better comparison and showing power consumption importance at low voltages. Section 2 introduces design of full adders. Section 3 demonstrates circuits of the three full adder modules. Section 4 discusses simulation to select a superior structure and to present the results. Section 5 presents an overall conclusion on the activities performed in this paper.

2. Full Adder Design

Figure 1 shows the diagram of an XOR-XNOR-based 1-bit full adder. The circuit consists of three major modules. Since the modules may be implemented using various methods and logics, a full adder circuit can be designed using different forms and logics. In this figure, A and B are the inputs, C_{in} is the input Carry, and Sum is total and C_{out} is the output Carry. Expressions (1) and (2) present the relationship between the inputs and outputs [2].

$$S = A \oplus B \oplus C_{in} \quad (1)$$

$$C_{out} = A.B + A.C_{in} + B.C_{in} \quad (2)$$

The Boolean expression in (1) and (2) may be arranged by the following expressions.

$$H = A \oplus B \quad (3)$$

$$Sum = H \oplus C_{in} = H.\overline{C_{in}} + \overline{H}.C_{in} \quad (4)$$

$$C_{out} = A.\overline{H} + C_{in}.H \quad (5)$$

Expressions (4) and (5) show, H and its complement H' are the preliminary variables for Sum and C_{out}, H and H' should be produced in the module I, which are used in module II with C_{in} for creating C_{out}. Module III was used for producing C_{out} using H, H', A, and C_{in} outputs [3]. According to the study of all full adders at sub-threshold voltages, attempts were made here not to use NOT gates as much as possible to reduce power consumption whose major factor at low voltages is leakage power. Therefore, the circuits are used for module I, which create H and H' signals simultaneously without needing a NOT gate. A NOT gate usually need for producing H' signal in XOR-XOR-based or XNOR-XNOR-based adder structures, at the following discusses XOR-XNOR-based adders. Sum and Carry outputs are produced using expressions (4) and (5) in all the XOR-XNOR-based adders. In this full adder, module I includes an XOR-XNOR circuit that generates H and H' signals. Modules II and III include, 2-to-1 multiplexers with select lines of H and H' or C_{in} and C_{in}', which generate Sum and Carry outputs, respectively. Simultaneous generation of H and H' signals in full adders is important as they drive select lines of output stage of multiplexers. In another case (non-simultaneous H and H'), there may be glitches and unnecessary power dissipation may occur. The final outputs cannot be generated until these intermediate signals are available from module I.

3. Full Adder Building Blocks

XOR and XNOR gates play a crucial role in different circuits, especially computational circuits and their optimal design improves efficiency of the circuits. According to the importance of designing and manufacturing full adders, it is necessary to discuss XOR and XNOR circuits design because they have been considered as the most fundamental element in designing this level of circuits. Simultaneous generation of XOR and XNOR has been used recently for module I extensively [4, 5]. This feature is extremely favorable as output signals are generated in the module for driving select lines of a multiplexer in a full adder. Figure 2 shows the 2-to-1 multiplexer circuit for module III. Output of the module can be expressed as (5). Figure 3 shows all the circuits that have been designed already for module I. Figure 4 shows some frequently used circuits that have been presented already for module II. The circuits necessarily perform XOR or XNOR and they can be used in adder module I; however, they cannot have an appropriate performance in that module.

4. HSPICE Simulation and Results

HSPICE and 90 nm IBM library were employed here for performing simulations. V_{DD}=1.2V was used for nominal value of the voltage source. The results were presented for module I and module II in voltage sources of V_{DD}=220mV and V_{DD}=310mV, respectively.

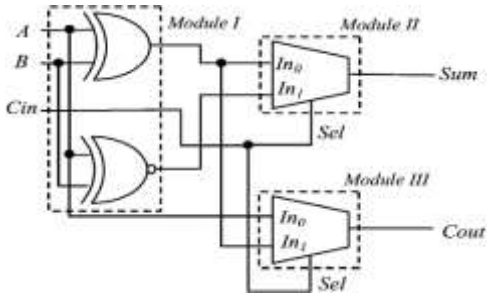


Figure (1) General form centralized full adder

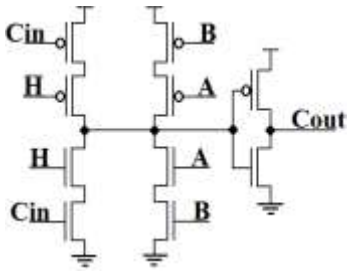
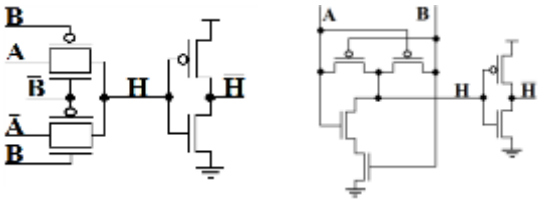


Figure (2) Circuit for module III [2]



A B

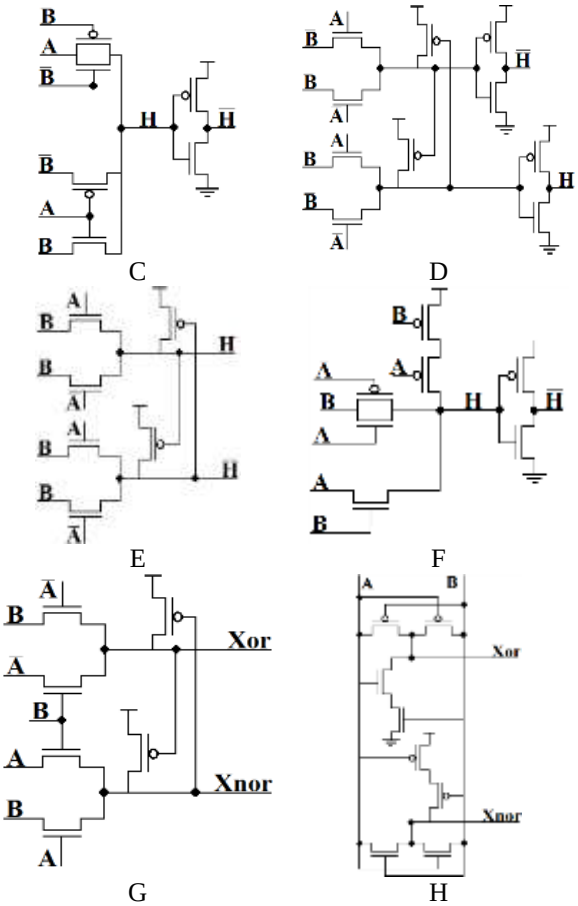
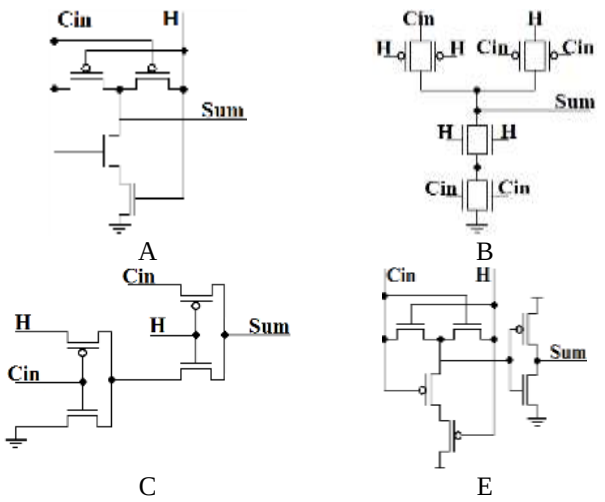


Figure (3) Existing circuits for module I



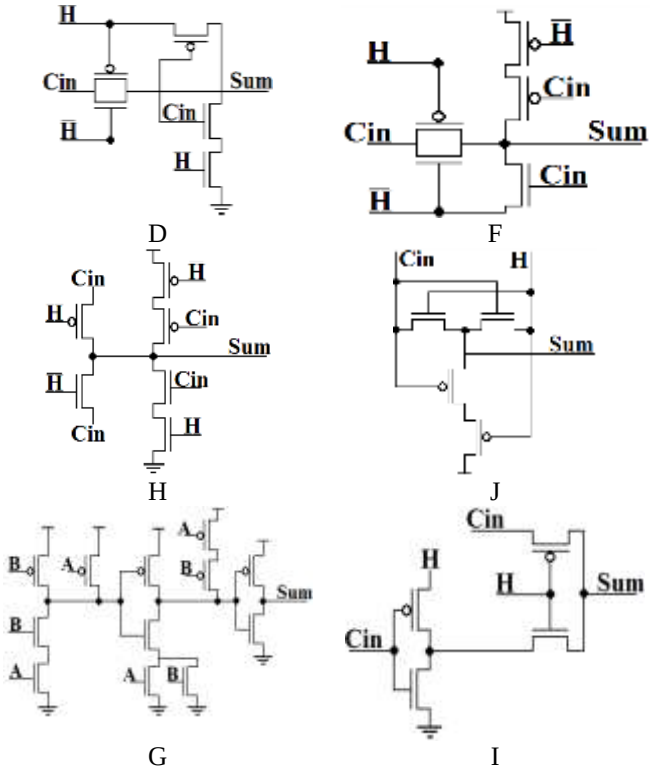


Figure (4) Existing circuits for module II

V_{DD}=260mV voltage source was used for comparing the full adders (considered values of V_{DD} are minimum voltages that the all of simulated circuits have operated well).

Input and output buffers were used for all inputs and outputs to simulate a real environment. Figure 5 shows the test structure for general simulation and size of transistors in each buffer. Size of transistors of these buffers is selected in a way that there is sufficient expected signal distortion in a real circuit.

In order to have a fair comparison, all the simulated circuits are prototyped at minimum transistor sizing. The transistor sizes of all the simulated circuits have been included in the figures. In the circuits, the numbers depict the width (W) of the transistors with the minimum feature size as 2λ. All the circuits have been sized to achieve best PDP.

Inputs of a 1-bit full adder (A, B, and C_{in}) may change into 56 different modes. That is, three inputs of a 1-bit adder may represent 8 binary figures as "000" to "111". Each eight binary figure ("000" to "111") should spring into all figures except itself. Therefore, there are seven springs for each eight binary figure. Consequently, all possible mode changes equal 8×7=56. This method was used for simulation of all modules.

An input transition may or may not result in change at the output node. Even if there is no switching at the output node, some internal node may be switching. This switching activity results in some power dissipation. For an accurate result, all the possible input combinations are considered for all the test circuits. Figure 6 shows the output waveforms and input stimulus used for the full adder circuits.

Performances of the full adder circuits and the proposed modules were evaluated in terms of the worst delay mode, power consumption, PDP, P^2DP, in 10MHz frequency.

The delay is calculated from 50% of the input voltage level to 50% of the output voltage level obtained from all the rising and falling output transitions. In order to calculate the delay in the worst condition, all the 56 modes should be examined to measure the delay of all output mode changes (C_{out} and Sum) and introduce the biggest delay as the worst delay [2].
Tables 1 and 2 show the simulation results related to studying the circuits shown for module I and module II such as of delay, power consumption, PDP, and P^2DP. The results show that circuit H is the superior structure of module I and H and F circuits are the superior structures for module II. Figure 7 shows the two new structures of full adders, which were designed using the modules.

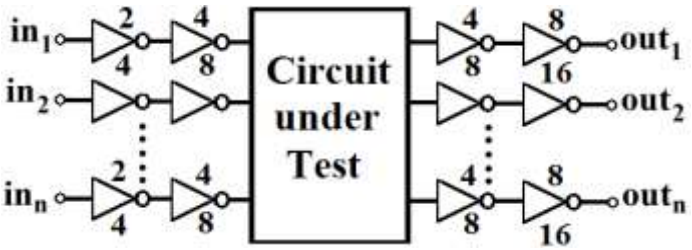


Figure (5) Simulation test bench

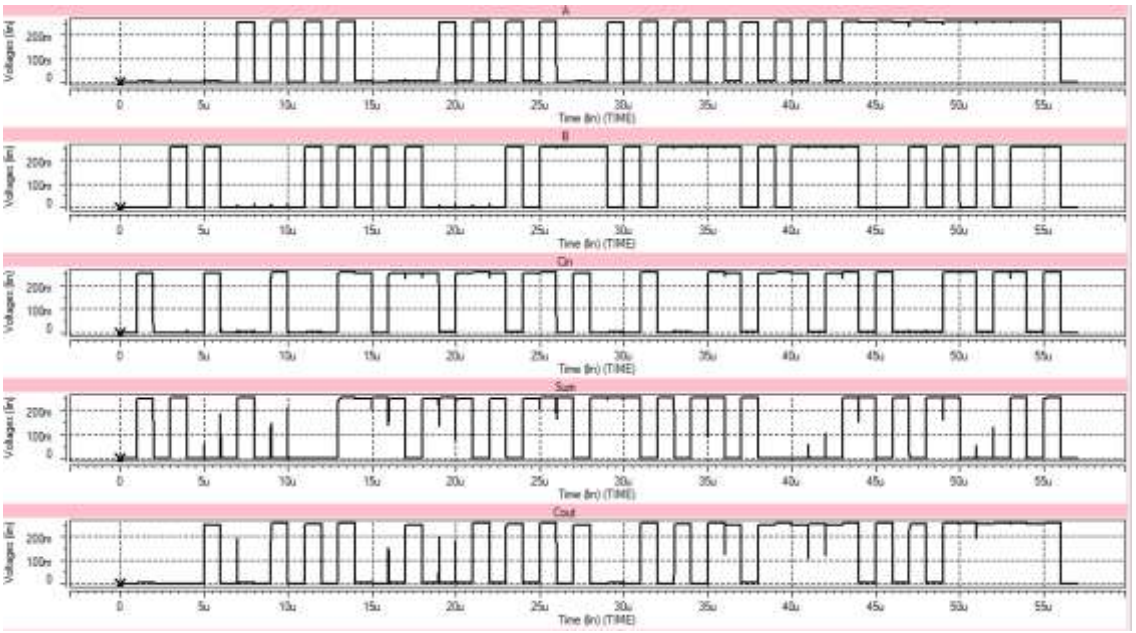


Figure (6) Output signals and input stimulus used for the full adder circuits

Table 1- Module I HSpice Simulation Results at 90nm, V_{DD}=220mV

Circuit	No. of Tr.	Power (nW)	Delay(nS)		PDP (aJ)	P^2DP
			Xor	Xnor		
A	10	13.56	9.39	12.09	164.06	2.225
B	6	12.39	9.20	16.02	198.51	2.459
C	8	13	9.18	12.16	158.17	2.056
D	14	14.89	10.88	9.69	162.07	2.413
E	10	13.84	7.77	8.22	113.9	1.576
F	9	13.14	11.88	9.01	156.2	2.053
G	8	13.30	11.08	13.39	178.2	2.372
H	8	13	10.13	7.762	131.8	1.714

Table 2- Module II HSpice Simulation Results at 90nm, V_{DD}=310mV

Circuit	No. of Tr.	Power (nW)	Delay (nS)	PDP (aJ)	P^2DP
A	4	13.823	2.219	30.68	4.240
B	8	14.253	2.076	29.59	4.217
C	4	13.053	3.139	40.97	5.348
D	5	9.611	11.506	110.58	1.062
E	6	14.884	3.136	46.68	6.948
F	4	9.4007	10.287	96.706	0.909
G	12	16.728	5.880	98.36	16.453
H	6	9.752	11.33	110.51	1.077
I	4	15.042	3.006	45.22	6.802
J	4	13.96	2.058	28.73	4.011

Table 3, shows the simulation results of the common full adders and two proposed full adders in terms of number of transistors, power consumption, delay, PDP and P^2DP at V_{DD}=260mV. A comparison between the results of Table 3 has been shown in Figure 8 to 10. Moreover, Table 4 shows the PDP improvement of proposed full adders.

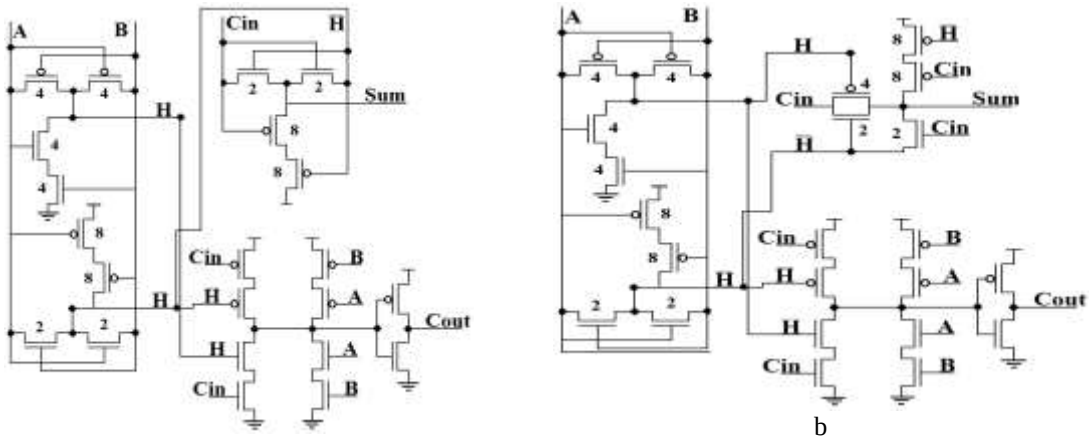


Figure (7) Proposed 1bit-full adder circuits, (a: Proposed Circuit-I, b: Proposed Circuit-II)

Table 3- Full adder HSPICE simulation results at 90 nm, VDD=260mV

Full Adder	No. of Tr.	Power (nW)	Delay(nS)		PDP (aJ)	P^2DP
			Sum	Cout		
CMOS	28	24.14	15.80	9.52	381.6	9.21
New Hybrid CMOS	24	24.43	16.14	12.39	394.5	9.64
HPSC	22	24.44	25.57	13.74	599.6	14.06
DPL	28	24.29	12.07	11.65	293.1	7.12
FA in [6]	16	24.78	13.21	11.91	327.4	8.11
FA in [7]	18	21.55	14.96	10.26	322.5	9.95
FA in [8]	19	22.107	16.44	10.96	363.6	8.03
Proposed I	22	23.48	9.57	11.58	272.1	6.39
Proposed II	23	23.52	10.53	12.82	274.2	6.49

Table 4- Improvement of the Proposed Full Adders

FA	Improvement (PDP) of Proposed-I Circuit	Improvement (PDP) of Proposed-II Circuit
CMOS	29%	28%
New Hybrid CMOS	31%	30%
HPSC	55%	54%
DPL	8%	6%
FA in [6]	19%	16%
FA in [7]	16%	15%
FA in [8]	25%	24%

It is apparent that amongst the existing conventional full adders, the adders without driving capability (TGA) and CPL have the smallest delays. This can also be observed from Table 3 as DPL and FA in [8], are amongst the faster adders. The Proposed Circuits full adder follow the DPL and HPSC adders. Among the nonconventional or hybrid full adders, the proposed hybrid full adder shows minimum delay at 260mV V_{DD}, when compared to the CMOS, HPSC, Hybrid CMOS and DPL full adders. At V_{DD}=260 mV, the proposed adders are 24%, 53%, 25%, and 28% faster than CMOS, HPSC, Hybrid CMOS and Hybrid full adders, respectively. Among the conventional existing full adders, clearly New Hybrid CMOS has the highest power dissipation[11]. The New Hybrid CMOS adder dissipates the most power because of its dual-rail structure and high number of internal nodes in its design. Therefore, the New Hybrid CMOS topology should not be used if the primary target is low power dissipation. Among the nonconventional or hybrid-CMOS full adders, the proposed full adder and Full Adder in [7], have the least power dissipation. The PDP is a quantitative measure of the efficiency of the trade off between power dissipation and speed, and is particularly important when low-power operation is needed. Among conventional adders, the adders CMOS and DPL have the lowest PDP. In the case of nonconventional or hybrid-CMOS adders, the proposed hybrid full adder displays the best PDP characteristics for supply voltage 260mV. Figure 8 to 10 shows the full adder circuits which are presented in [2], [6] and [7].

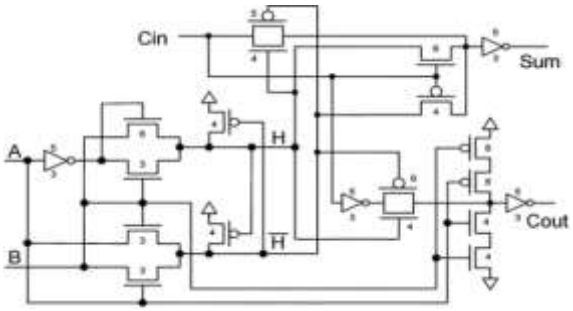


Figure (8) Full adder circuit proposed in [2]

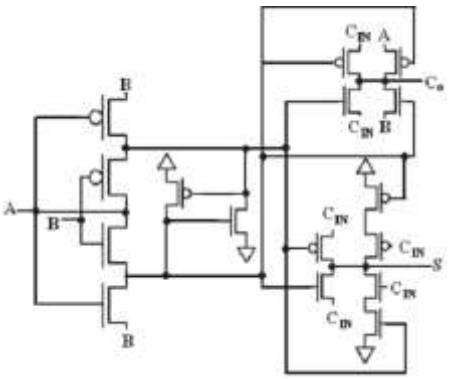


Figure (9) Full adder circuit proposed in [6]

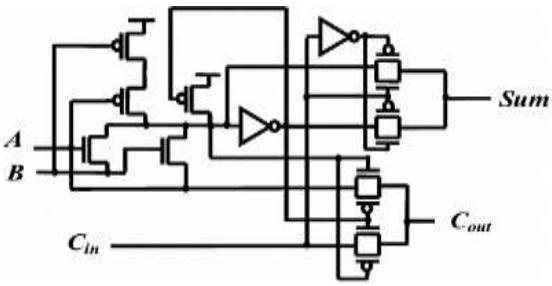


Figure (10) Full adder circuit proposed in [7]

5. Conclusions

This paper presents two new full-adder circuits suitable for sub-threshold voltage technology. These new structures are obtained by selection of the best circuits of module I and module II (the basic building blocks of a full-adder circuit). The proposed-I and proposed-II full adders outperform their counterparts showing at least 55% and 54% improvement in power-delay product, respectively.

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