

Design of New Full Swing Low-Power and High-Performance Full Adder for Low-Voltage Designs

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Abstract

This paper, presents a new design for 1-bit full adder cell using hybrid-CMOS logic style. The new full swing full adder cell has excellent performance in low values of power supply, so this circuit is a suitable choice for low-power applications and low-voltage designs. According to the simulation results, the proposed full adder has the best power consumption, propagation delay and power-delay product compared to its counterparts, such that the power-delay product of the proposed full adder is 39% better than the next best PDP. HSPICE simulations using TSMC's 130nm technology with a power supply of 1.2V was utilized to evaluate the performance of the circuits.

Keywords: Full Adder, High-Performance, Hybrid-CMOS, Low-Power, Low-Voltage, VLSI

Introduction:

The Most of the VLSI applications, such as digital signal processing, image processing, and digital filter design, widely use arithmetic operations. Addition, subtraction and multiplication are examples of the most commonly used operations. The 1-bit full adder cell is the building block of these units. Hence, improving its performance is critical for improving the overall unit performance. The most important performance parameters for a generic VLSI system are power consumption, speed, and chip area.

Several logic styles have been used in the past to design full adder cells. Each logic style has its own advantages and disadvantages. Classical designs of full adders normally used only one logic style for the whole full adder design. Standard static CMOS, members of pass-transistor logic (PTL) family such as CPL, DPL, SRPL, and transmission gate are the most important logic styles in the conventional full adders [1].

In the other full adder designs, more than one logic style have been used. These designs are called hybrid-CMOS logic style [2]. These designs use the features of different logic styles to improve upon the performance of the designs using single logic style. HPSC full adder (hybrid pass logic with static CMOS output drive full adder) [3], New-HPSC adder [4], New-Hybrid-CMOS adder [5], and full adders proposed in [2] and [6] are the examples of adders designed with this logic style.

In this paper, a novel 1-bit full adder has been proposed with better performance in comparison with these existing full adders. Some of the most famous of them are shown in Figures 1 to 3.

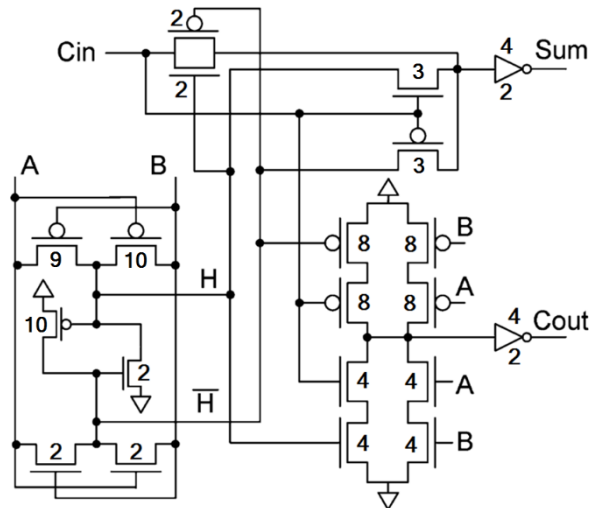


Figure (1) HPSC full adder cell

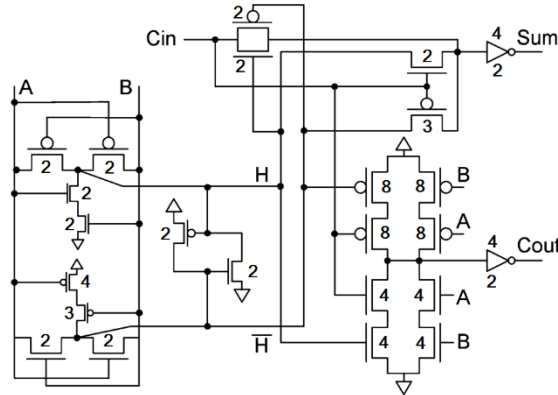


Figure (2) New-HPSC full adder cell

The rest of this paper is organized as follow, in section 2, power consumption issues in CMOS VLSI circuits will be discussed. In section 3, the main structure of a 1-bit full adder will be introduced. Then in section 4, the proposed 1-bit full adder will be introduced. In section 5, simulation environment will be described and in section 6 simulation results will be proposed, which show the supremacy of the proposed cell. Finally, in section 7, the paper will be concluded.

2. Power Consumption in VLSI Circuits

There are three main components of power consumption in digital VLSI circuits.

- 1) *Switching component: consumed in charging and discharging of the circuit capacitances during transistor switching.*
- 2) *Short-circuit component: Created by short-circuit current flowing from supply voltage to ground during transistor switching.*
- 3) *Static power component: Existence of static and leakage currents in stable state of circuit cause this component of power consumption.*

The first two components are referred to as dynamic power, since power is consumed dynamically while the circuit is changing states [7]. Dynamic power accounts for the majority of the total power consumption in digital VLSI circuits [8]. It depends on the input pattern applied to the circuit, which will either cause the transistors to switch or to keep their previous state at each clock cycle [7]. The third component is usually negligible in a well-designed CMOS circuit [8].

The total power is given by

$$P_{total} = V_{dd} \cdot f_{clk} \cdot \sum_i V_{swing} \cdot C_{load} \cdot p_i + V_{dd} \cdot \sum_i I_{i-sc} + V_{dd} \cdot I_l \quad (1)$$

where V_{dd} is the supply voltage. V_{swing} is the voltage swing of the output which is ideally equal to V_{dd} . C_{load} is the load capacitance at node i . f_{clk} is the system clock frequency. p_i is the switching activity at node i . I_{i-sc} is the short-circuit current at node i and I_l is the leakage current [7].

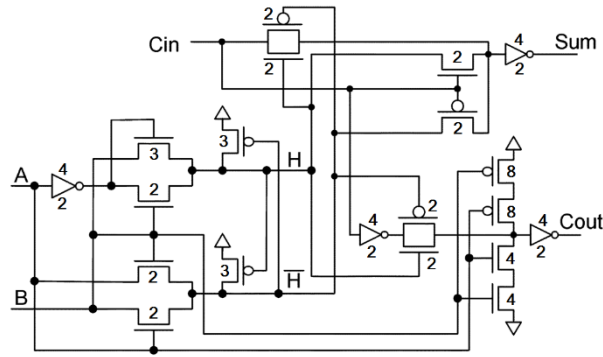


Figure (3) New-Hybrid-CMOS full adder cell

Reducing the number and magnitude of the circuit capacitances, reducing the voltage swing at some internal nodes, and reducing the spurious transitions in the output signal are some of techniques used at the circuit level to reduce the power consumption [7].

3. Main Structure of 1-Bit Full Adder

Generally, hybrid-CMOS full adders are categorized in three groups depending on their structure and logical expression of Sum output [5]. The first category of full adders is based on XOR gates and second one is based on XNOR gates. In third category, the Sum and Carry outputs are generated by XOR-XNOR intermediate signals [2]. In this paper, the proposed full adders stand on third category.

The Sum and Carry (C_{out}) outputs of a 1-bit full adder generated from the binary inputs A, B, and C_{in} can be generally expressed as

$$SUM = A \oplus B \oplus C_{in} \quad (2)$$

$$C_{out} = A.B + C_{in} (A \oplus B) \quad (3)$$

In third category, the Sum and Carry outputs are generated by the following expression, where H is the XOR of A and B, and H' is the complement of H

$$SUM = H \oplus C_{in} = H.C'_{in} + H'.C_{in} \quad (4)$$

$$C_{out} = B.H' + C_{in}.H \quad (5)$$

Generally, this category is divided by three modules. Module I is a XOR-XNOR circuit producing H and H' signals. Module II and III produce Sum and C_{out} as outputs, respectively. Module II and III are 2-to-1 multiplexers with H and H' as select lines. The simultaneous generation of H and H' signals is critical in these types of adders, because they drive the select lines of the multiplexers in the output stage. Otherwise, there may be glitches and unnecessary power dissipation may be occur [2].

4. Proposed Full Adder

The main structure of 1-bit full adder introduced in section III. As mentioned in the previous section, the proposed full adder stands on third category. This is shown in Figure 4.

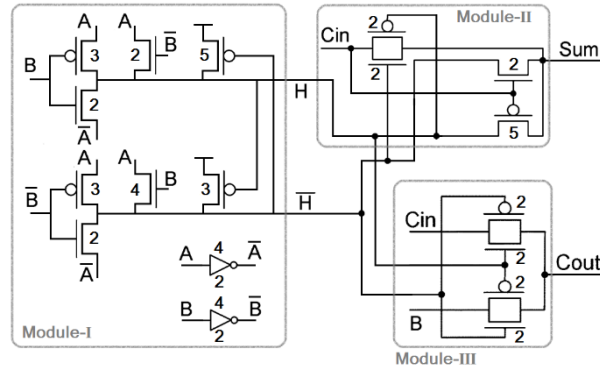


Figure (4) Proposed full adder cell

The intermediate signals H and H' are produced by module I, which has been implemented by a novel structure. This module is an XOR/XNOR gate that produces the intermediate signals H and H' simultaneously. Module II is an XOR gate similar to that used in HPSC, New-HPSC and New-Hybrid-CMOS full adders and generates Sum as output. Module III is a multiplexer with H and H' as select lines, and produces the Carry output signal.

5. Description of Simulation Environment

HSPICE simulations using TSMC's 130nm technology with a power supply of 1.2V was utilized to evaluate the performance of the circuits. Furthermore, simulations carried out in all process corners (TT, SS, SF, FS and FF).

To simulate a real environment, input buffers for all inputs of the test circuit are used. The transistor sizes of these buffers are chosen such that there is sufficient signal distortion as expected in an actual circuit. A minimum output load of fan-out of four inverters (FO4) is used for power and delay measurements [5], the value of which amounts to 4.704fF (1.176fF for each inverter in TSMC's 130nm technology). The generic simulation test bench used is shown in Figure 5, along with the transistor sizes of each buffer [2]. To reach more accurate results, all transitions from an input combination to another (56 patterns) have been tested, and the delay at each transition has been measured. The maximum has been reported as the cell delay. Figure 6, shows the output signals and input stimulus with maximum frequency of 50MHz used for the full adder circuits. The average power for the duration of this pattern has been reported as the cell power consumption figure.

The transistor sizes of all the simulated circuits have been included in the figures. In the circuits, the numbers depict the width (W) of the transistors with the minimum feature size as 2λ .

All the circuits have been sized to achieve best power-delay product (PDP).

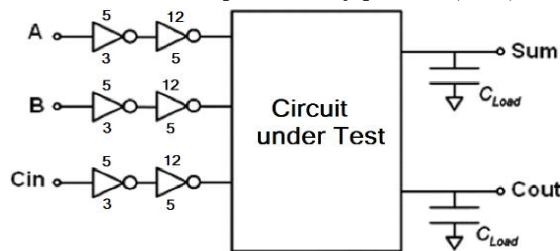


Figure (5) Simulation test bench [5]

For the calculation of power-delay product, worst-case delay is chosen to be larger delay amongst the two outputs.

6. Simulation Results

In this section, simulation of full adder cells is presented under the mentioned conditions in previous section. The circuit performance of the test circuits is evaluated in terms of worst-case delay, power dissipation, and power-delay product at 1.2V supply voltage. The simulation results are shown in Table 1. According to the results, the proposed full adder is the best structure in terms of power consumption and propagation delay. The proposed full adder consumes 9% less power than FA proposed in [6], 11% less than New-Hybrid-CMOS, 15% less than New-HPSC, 16% less than FA proposed in [2], and 30% less than HPSC.

In addition, the proposed adder has 28% less delay than New-HPSC, 32% less than New-Hybrid-CMOS, 34% less than FA proposed in [2], 42% less than HPSC, and 55% less than FA proposed in [6]. As can be seen, delay improvement of the proposed full adder is more than improvement for power consumption, compared to its counterparts.

In order to excellence of both power consumption and delay of the proposed full adder, we can say that the proposed adder has the best PDP compared to its counterparts. Table 2 shows the PDP improvement of the proposed full adder compared to other full adders for all process corners.

According to the Table 2, PDP improvement is from 39% compared to New-Hybrid-CMOS to 59% compared to HPSC full adder for TT process corner. Moreover, the proposed full adder has the best performance in terms of power consumption, delay and PDP in other process corners, compared to its counterparts.

The simulation results for power consumption, propagation delay and PDP have been depicted in the Figures 7, 8, and 9, respectively for all process corners.

Moreover, the values of power consumption, delay, and PDP for a range of supply voltages (1.2-0.6 V) are shown in Figures 10 to 12, respectively.

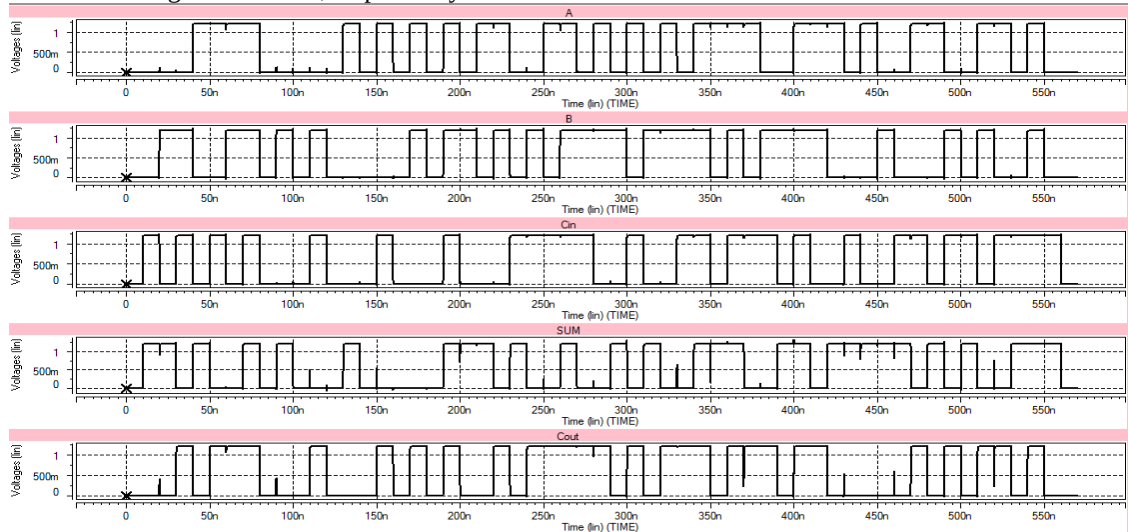


Figure (6) Input stimulus used for the full adder circuits and output signals

Table 1-Simulation result for six 1-bit full adder cell in TSMC's 130nm technology with $V_{DD}=1.2V$

FA	TT			SS			SF			FS			FF		
	Pow (μW)	Delay (ps)	PDP (fJ)	Pow (μW)	Delay (ps)	PDP (fJ)	Pow (μW)	Delay (ps)	PDP (fJ)	Pow (μW)	Delay (ps)	PDP (fJ)	Pow (μW)	Delay (ps)	PDP (fJ)
HPSC	3.79	266.2 6	1010. 1	3.70	409.2 9	1516. 4	3.73	356.2 9	1328. 9	4.03	380.4 8	1533. 4	3.99	197.2 8	786.5 8
New HPSC	3.17	216.6 3	686.4 2	3.07	273.5 1	839.2 6	3.15	221.5 3	697.6 9	3.24	223.9 6	726.6 9	3.35	180.1 2	602.9 4
New Hybrid CMOS	3.01	226.9 7	682.5 3	2.89	284.5 4	823.8 6	3.06	252.2 2	770.8 8	3.03	228.3 5	692.3 6	3.19	189.6 3	605.4 5
FA in [2]	3.20	233.3 0	747.6 1	3.08	288.6 7	889.3 8	3.14	227.9 7	715.3 8	3.25	244.3 7	795.5 5	3.41	191.9 4	653.9 4
FA in [6]	2.95	340.8 3	1004. 5	2.85	565.9 6	1615. 4	3.02	277.6 2	837.4 6	2.94	467.5 5	1375. 4	3.09	229.0 4	707.2 4
Proposed FA	2.68	154.7 1	414.9 0	2.63	188.3 2	495.2 7	2.71	165.5 4	448.5 3	2.76	163.9 0	452.2 1	2.81	128.2 3	360.6 5

Table 2-PDP improvement of the proposed full adder compared to other full adders for all process corners

FA	HPSC	New HPSC	New Hybrid CMOS	FA in [2]	FA in [6]
TT	59%	39.5%	39%	44.5%	58.5%
SS	67%	41%	40%	44%	69%
SF	66%	35.5%	42%	37%	46.5%
FS	70.5%	38%	34.5%	43%	67%
FF	54%	40%	40.5%	45%	49%

As can be seen, the proposed full adder is the best structure in terms of power consumption at all values of supply voltage except 0.6V that the FA proposed in [6] has least power consumption in that voltage. However, the proposed full adder has the best performance in terms of delay and PDP at all values of supply voltage. So the proposed full adder is a proper choice for low-voltage designs.

7. Conclusions

A novel full swing low-power 1-bit full adder has been proposed. Low power consumption is targeted at the circuit-design level. The simulation results indicated that the proposed full adder has minimum delay and PDP for all values of supply voltage compared to its counterparts. So that is a proper choice for low-power and low-voltage designs.

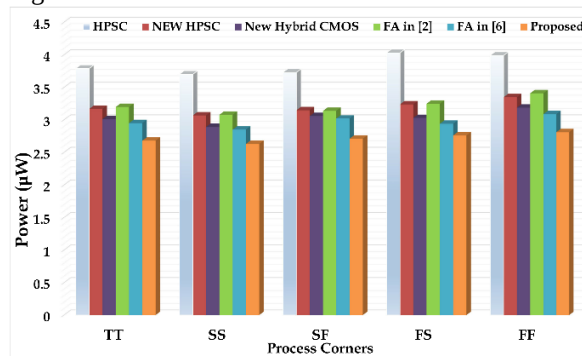


Figure (7) Simulation result for power consumption in TSMC's 130nm technology with $V_{DD}=1.2V$

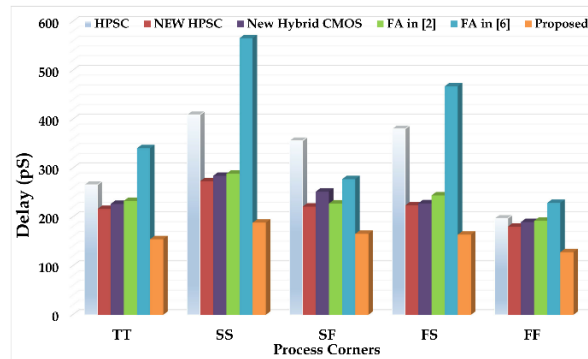


Figure (8) Simulation result for propagation delay in TSMC's 130nm technology with $V_{DD}=1.2V$

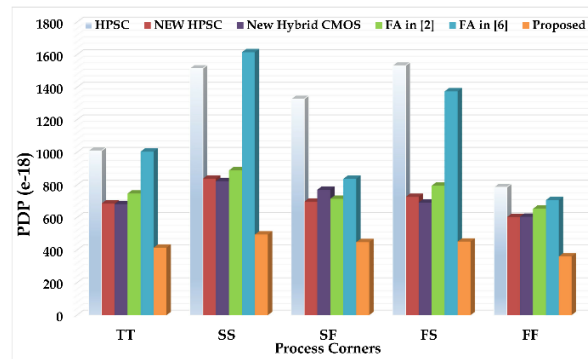


Figure (9) Simulation result for PDP in TSMC's 130nm technology with $V_{DD}=1.2V$

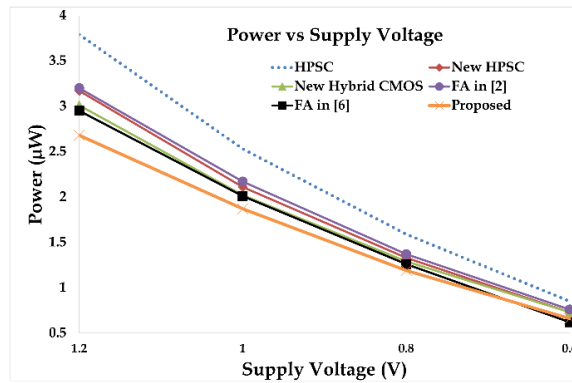


Figure (10) Power consumption results for different supply voltages

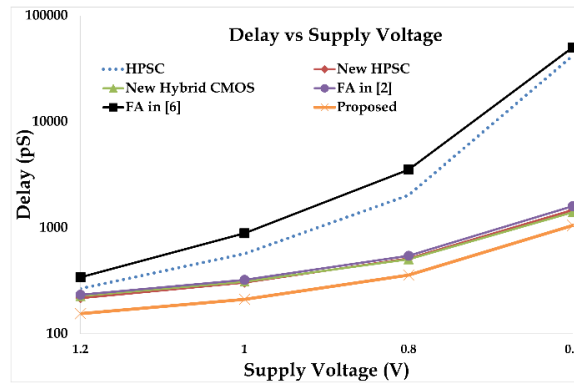


Figure (11) Propagation delay results for different supply voltages

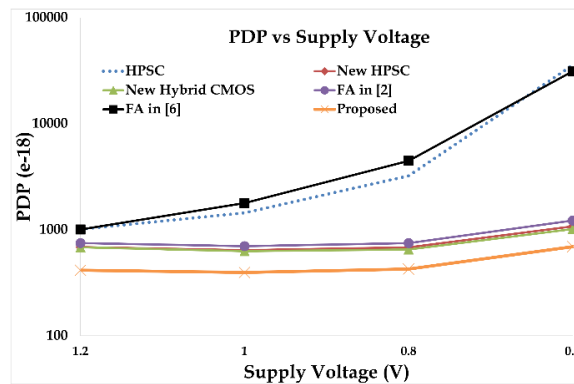


Figure (12) PDP results for different supply voltages

Moreover, the proposed full adder has the best performance in terms of power consumption, delay and PDP in other process corners, compared to its counterparts.

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