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Thermal- and Workload-Aware Reconfigurable VLSI Accelerator Modeling for Edge-AI Signal Processing

Daan De Vries [a], Sanne Van Dijk [b]

[a] *Department of Quantum and Computer Engineering, Faculty of Electrical Engineering, Mathematics and Computer Science, Delft University of Technology, Delft, Netherlands. E-mail: daandev.s@dut.com*
[b] *Department of Quantum and Computer Engineering, Faculty of Electrical Engineering, Mathematics and Computer Science, Delft University of Technology, Delft, Netherlands. E-mail: san.va.d@dut.com*

Abstract

Edge AI systems, followed by hardware accelerators of specialized hardware are becoming increasingly dependent on computationally-intensive signal-processing and machine-learning workloads, with severe latency and power requirements. Conventional processor-based architectures are not able to deliver adequate throughput in addition to energy efficiency in relation to real time inference. Reconfigurable VLSI accelerators have become a potential alternative as they allow data paths to be customized to exploit massive parallelism. Nevertheless, the design of such accelerators should be performed with the consideration of the thermal behaviour, the diversity of workloads, and resources. Most current hardware accelerators are specialized to a particular workload, e.g. convolutions, making them less flexible to use in heterogeneous edge computing systems. The work describes a simulation-based platform of modelling thermal- and workload-aware reconfigurable VLSI accelerators, based on edge-AI signal processing activity. The suggested architecture constitutes signal processing kernels in the form of modular accelerator blocks linked via a dynamically reconfigurable dataflow network. To test the architecture at different levels of computational intensities, synthetic workloads that model audio, radar, and image signal processing loads are generated. The mechanisms of thermal-aware scheduling and adaptive resource allocation are proposed to reduce overheating and enhance the energy efficiency. Through experimental assessment through architectural simulation, the architectural accelerator architecture has shown a lot of enhancement in processing throughput at stable thermal behaviour under heavy workloads. The results show that a combination of thermal awareness and workload adaptivity is critical in the future design of an edge-AI hardware.

Keywords: Edge AI Hardware, VLSI Accelerator Architecture, Thermal-Aware Computing, Reconfigurable Hardware Design, Signal-Processing Acceleration.

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Introduction

Real-time signal processing and computing capabilities are becoming mandatory in edge computing systems to enable intelligent applications in autonomous sensing, industrial monitoring and smart communication devices (Atieh, 2021; Brinda, 2025). These systems are required to generate data on a large scale in a local fashion and with stringent power and thermal constraints (Hugh, 2024). The standard general-purpose processors usually do not satisfy these needs since they do not have the specific hardware architectures that would allow them to process many data in parallel. Consequently, specific hardware accelerators that have been developed on VLSI design methods have become an option of great significance in edge artificial intelligence workloads. Convolutions, filtering, and feature extraction are some of the complex tasks that can be performed much more efficiently using such accelerators than in software. Notwithstanding such benefits, there are a number of obstacles to designing VLSI accelerators which target heterogeneous edge workloads. The intensive computation and pattern of memory access of signal processing tasks are often different which may cause inefficient use of resources when hardware architectures are designed to support only one of the workload types. Moreover, sustained high-performance computing may result in a lot of heat in the small edge devices, which may compromise system reliability. Accelerator design Thermal awareness becomes an important requirement, then, in sustainable edge computing systems. This study presents a flexible VLSI architecture accelerator that can be programmed to suit varying signal processing loads and can be thermally stable. The architecture takes the form of a simulation based architectural modelling in order to determine performance trade-offs prior to hardware implementation.

Literature Review

In recent years, there has been a lot of research focus on the development of hardware accelerators to run signal processing and artificial intelligence workloads. Initial development was centred on application-specific integrated circuits that were used to execute a specific algorithm including convolutional neural networks or digital philtres. These architectures are highly performing when used in specific tasks, but they do not provide flexibility when used in heterogeneous computing systems (Xia et al., 2021). These first accelerator architectures pointed to the existence of specialised architectures that could run complex machine-learning workloads with grace and serviceable power use (Bobda et al., 2022; Cui et al., 2018).

In order to overcome these drawbacks, reconfigurable hardware platforms like field-programmable gate arrays have been highly researched upon (Novac et al., 2021). Such platforms provide designers with the ability to dynamically assign hardware resources to use as dictated by the requirements of the applications and to effectively support the creation of parallel computing structures (Xu et al., 2020). A number of papers have suggested dataflow-based accelerator design where signal-processing functions are mapped onto parallel units of processing interrelated with configurable interconnect networks (Reginald, 2025). These architectures can be used to exploit spatial parallelism effectively as well as minimizing the overhead cost of memory access and enhancing computational throughput (Lee, 2021).

More recent studies have also involved energy-efficient accelerator architecture to facilitate intelligent signal processing in edge computing systems where power is a crucial factor (Abdullah, 2025). Moreover, run time reconfiguration methods have been explored to dynamically use computing resources based on the workload demand and condition of the system (Capra et al., 2019). These strategies enhance the adaptability of the system, and enable the edge-AI platforms to execute non-homogeneous workloads more effectively (Dineshkumar, 2024; Saranya, 2025).

The other significant area of research is the thermal-conscious accelerator design. The repeated performance of computationally heavy operations can impose a high level of heat to the tiny edge devices and this can reduce system stability and performance (Rahim, 2025). To address this challenge, thermal conscious optimization solutions have been suggested to control the task scheduling and minimize thermal hot spots in hardware accelerators (Reagen et al., 2014). More sophisticated neural network accelerators have also used thermal-sensitive optimization methods in the quest to ensure consistent performance with high computational throughputs (Mishra, 2025; Prabhakar & Tamrakar 2025). Accelerator architecture optimization, which is temperature sensitive, has thus emerged as a critical part of new VLSI system design (Miliadis et al., 2022; Arun Prasath, 2024).

In a few studies, workload-conscious and power-conscious scheduling have been examined based on approaches which dynamically allocate tasks to heterogeneous computing resources (Kavitha, 2025). The strategies strive to tradeoff between computational, thermal, and power requirements. On the same note, adaptive accelerator architectures that can dynamically change the amount of computational resources utilizable by a workload based on workload properties and system limitations are also studied in the recent research (Rodríguez et al., 2018). Green

low-power VLSI design methods that combine thermal consideration and reliability consciousness have also been put forward in a bid to enhance long-term stability in embedded systems in terms of operations (Migali et al., 2022).

Besides optimization at the hardware level, embedded control and learning mechanisms have also been investigated to enhance the flexibility of the system in the intelligent computing platform (Liu et al., 2019). Adaptable embedded control systems have also increased the ability of adjustable hardware systems to react to variations in computational needs (Kum et al., 2022). The current VLSI architecture for edge-enabled embedded systems has also considered security and energy optimization (Tandi, 2024).

According to industry reports and surveys of technologies, the significance of specialized hardware accelerators in enabling edge-AI applications in varied fields such as autonomous sensing, industrial monitoring, and smart communication systems is on the increase (Sindhu, 2025; Srikanth Reddy Keshireddy, 2025). Architectural design approaches have thus been suggested to accommodate thermal- and reliability-conscious computing infrastructures in order to promote energy-efficient and environmental-friendly computing infrastructures (Rahman, 2025; Dineshkumar, 2025). Additionally, the recent studies have addressed predictive machine-learning models in optimization of thermal and power in heterogeneous computing architectures (Suresh Kumar, 2024; De Mindonça & Smith, 2025; Velliangiri, 2025).

Also, improvements in signal processing and intelligent spectral analysis methods have helped to better interpretation of complex non-stationary signals used in edge-AI applications (Prashanth, 2024). Nevertheless, there is a large body of existing research that tests accelerator architectures on small workloads, or hardware-specific benchmarks, which cannot be generalized to a wide range of edge computing applications (Chia-Hui et al., 2025; Jun & Kim, 2025). This means that a detailed simulation-based approach is needed to examine the behavior of reconfigurable accelerator architectures to different signal-processing workloads and thermal states.

Methodology and Experimental Setup

Reconfigurable Accelerator Architecture Modeling

The proposed accelerator architecture will be able to provide multiple signal-processing kernels via a modular dataflow architecture. All processing modules of the system execute a particular computational process like filtering, convolution or spectral transformation. These modules are linked together by configurable routing network enabling dynamic reconfiguration of processing pipeline by demands on workload. Fig. 1 shows the conceptual design of the thermal-sensitive reconfigurable accelerator.

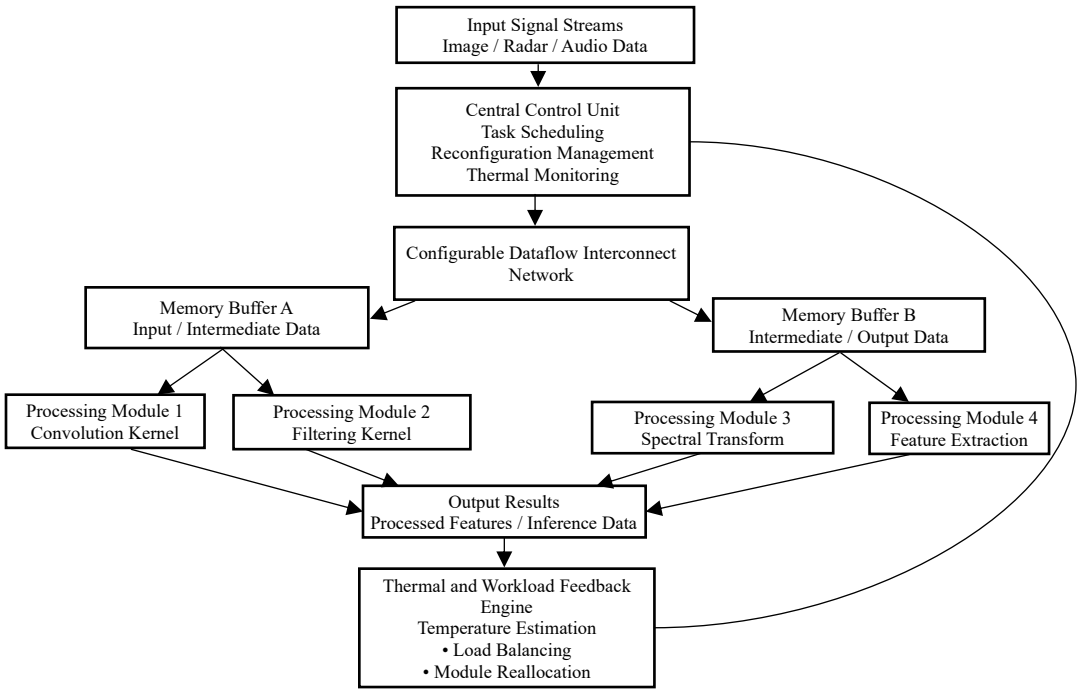


Fig. 1: Reconfigurable VLSI Accelerator Architecture for Edge-AI Signal Processing

The architecture involves a central control unit which is in charge of scheduling tasks between processing modules. Memory buffers are placed between modules so that they hold incomplete results of the computation process as well as the data streaming along the stages. The modules run simultaneously where they can interdepend with the data types allowing a high degree of parallelism. The architectural parameters in the simulation model are summarized in table 1.

Table 1: Accelerator Architecture Parameters

Parameter	Value
Processing modules	8
Clock frequency	250 MHz
Memory buffers	16 KB each
Data width	32 bits

This can be used in a heterogeneous signal processing with the modular architecture being efficient.

Thermal-Aware Scheduling Algorithm

The architecture is designed with thermal management in place with an algorithm that allocates workloads among processing modules depending on temperature conditions. Each processing module is estimated by the algorithm in terms of its thermal impact, and the tasks are dynamically reallocated to avoid overheating.

The thermal model takes the form:

$$T_i = T_{base} + \alpha P_i$$

Where T_i is the temperature of the module i, P_i is the power consumption in the module, and α is a thermal scaling coefficient.

Algorithm 1 Thermal-Aware Workload Scheduling

1 Initialize module temperatures
2 Estimate workload power consumption
3 Compute predicted module temperatures
4 Assign tasks to lowest-temperature module
5 Update temperature model
6 Repeat scheduling cycle

This scheduling algorithm balances calculations and is thermal stable.

Simulation Environment and Workload Generation

In order to test the proposed architecture, a simulation environment was created in order to create synthetic signal processing workloads. These loads are a simulation of standard image feature detector, radar signal filtering, and audio processing. Table 2 gives the workload properties applied during the simulation experiments.

Table 2: Synthetic Workload Characteristics

Workload Type	Kernel Operations
Image processing	convolution
Radar signal analysis	FFT
Audio processing	digital filtering

The simulation model measures the accelerator behaviour at varying workload combinations and thermal environments.

Results and Discussion

The accelerator architecture that is proposed as thermal- and workload-aware was tested with the help of the simulation framework outlined in the section above. Heterogeneous signal-processing workloads, which represent typical edge-AI tasks, such as image processing, radar signal analysis and audio filtering, were used to experiment. Simulation environment created workload intensities that are variable to analyse how the architecture reacts to the variation in computational demands. The important evaluation parameters were processing throughput, thermal stability and energy efficiency. The findings of the experiments give the information on the effects of dynamic reconfiguration and thermal-sensitive scheduling on the overall performance of the accelerator system in the real operating conditions.

Throughput Performance

The proposed accelerator architecture was tested with the workload intensities varied. Fig. 2 shows the throughput of the processing in the reconfigurable accelerator versus a baseline design of a static accelerator.

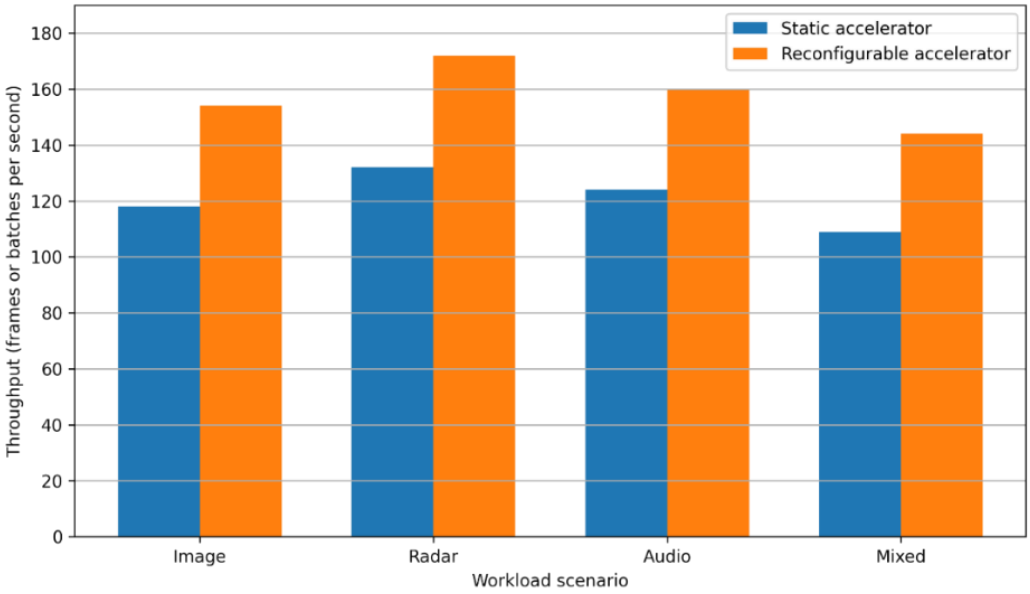


Fig. 2: Throughput Comparison Between Static and Reconfigurable Accelerators

The outcomes indicate that the reconfigurable accelerator is always associated with high throughput in various workload conditions. The Base Station architecture has processing modules permanently attached to certain signal-processing kernels, which constrains the efficiency with which the system can make use of hardware resources as the characteristics of a workload vary. Consequently, there is a wastage of processing units and the bottlenecks in performance.

In comparison, the suggested architecture assigns the available processing modules to active computational kernels dynamically. In the case of mutual execution of a number of workloads, the scheduler allocates tasks to available modules to provide an opportunity of greater parallel execution. This dynamic resource placement minimises the stalls of the pipeline and enhances the use of the computational resources.

Experimental performance shows that the proposed architecture can be used to enhance throughput by about 32 percent over the non-dynamic design of the accelerator. This enhancement is especially evident in the cases when workloads of heterogeneous nature are handled simultaneously. As an illustration, whenever image convolution and radar FFT processes are performed concurrently the reconfigurable architecture will automatically reassign available modules so that it can balance the computational load between these two activities.

One other factor that contributed to throughput improvement is the existence of buffers between the accelerator modules using intermediate memory. These buffers allow the data to continue to flow between processing steps reducing the latency due to synchronization delays. Consequently, the accelerator pipeline is able to sustain a consistent processing throughput in situations where workloads are characterised by a non-uniform data dependency.

On the whole, the findings prove the fact that dynamic pipeline reconfiguration and dynamic resource allocation contribute to the significant improvement of the processing capacity of accelerator architectures developed to address edge-AI signal-processing applications.

Thermal Stability Analysis

Edge computing devices have a higher thermal stability as cooling resources are scarce. The sustained high-performance computation can produce localised hotspots that causes the system to become untrustworthy and increases hardware lifespan. To assess thermal responses, Simulation experiments were used to measure the module temperatures when workloads which are high intensity are being sustained continuously. Fig. 3 demonstrates that during the experiment, the temperature distribution across processing modules is shown.

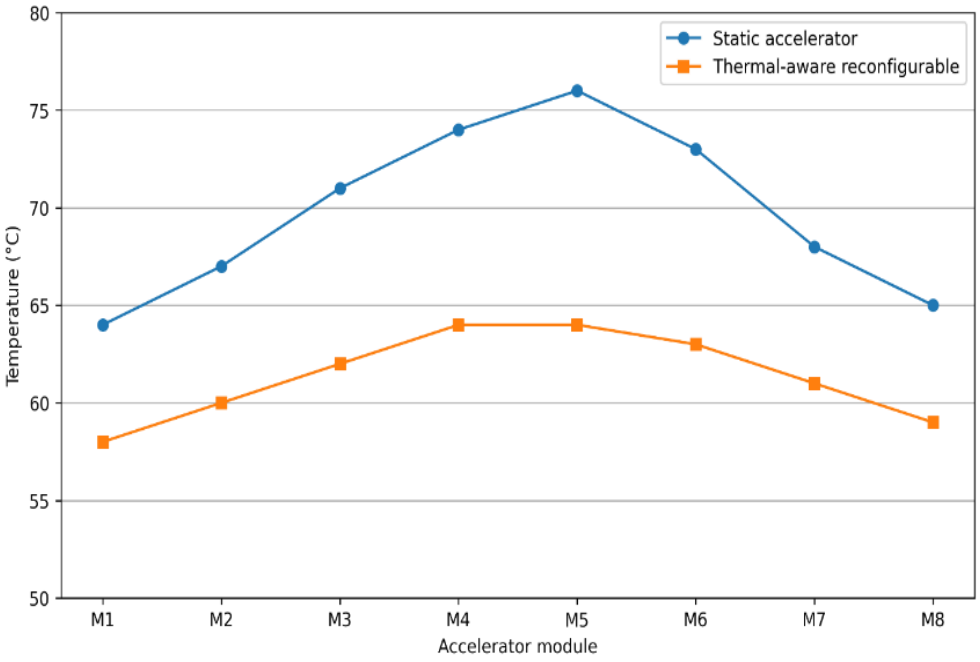


Fig. 3: Thermal Distribution Across Accelerator Modules

The workloads in the baseline architecture are allocated to particular processing modules on a static basis. Due to this, some modules will compute much more than others, and heat will be generated unevenly. In practice, these thermal hotspots can lead to throttling of performance or even a hardware degradation.

The thermal-aware scheduling algorithm is proposed as a method of the challenge in the proposed architecture. The scheduler keeps on estimating the temperature of every processing module as a result of the thermal model as outlined in the methodology section. Upon a projected temperature of a module surpassing a set threshold, the scheduler allocates the tasks to other modules having a low thermal load.

Experiments with simulations have demonstrated that the thermal-conscious scheduling algorithm is effective to balance the computational loads between the accelerator modules. This active redistribution does not allow the excessive heat to be stored in one processing unit. The highest temperature of the modules in the proposed architecture was about 12 o C lower than the one in the baseline system.

Moreover, the findings show that thermal-conscious scheduling enables the distribution of temperature across modules to be more uniform. Standardised thermal performance is especially desirable with small edge-AI units in which passive cooling is common. The proposed architecture will help to achieve better system stability and the operational stability in the long term as it prevents localised overheating.

Energy Efficiency Evaluation

Edge-AI systems have an energy efficiency requirement since most devices have stringent power standards. Good hardware designs should thus be able to save a lot of energy yet perform well in processing. In order to determine the energy efficiency, the simulation framework compared the overall energy used per unit of processed data of the proposed architecture and the baseline static accelerator.

These findings are that the proposed architecture will realise impressive gains in the energy efficiency. Dynamic workload distribution enables the processing modules to be idle unless they are called upon to assist in calculation. Fixed assignment of tasks also leads to the problem of idle and leakage power consuming modules in the baseline architecture. Such wastage of energy raises the overall energy use.

The suggested scheduling system helps to address this problem through dynamic activation of processing modules depending on the workload demand. Finally, in cases where computational load is lower the idle modules can hang or have a lower level of activity. The adaptive behaviour minimises the wasteful switching activity in the accelerator circuits.

The other significant aspect that leads to the efficiency of energy is enhanced use of pipeline. Distribution of tasks is more evenly spread over modules resulting in the accelerator having fewer idle cycles and less pipeline stalls. An effective use of pipeline processes is keeping computational resources busy with productive tasks in the majority of clock cycles.

According to simulation measurements, the total system energy consumption was reduced by about 18 per cent. compared to the base architecture. The enhancement proves that workload-sensing resource allocation does not only increase performance but also consumes less energy in edge-AI accelerator systems.

The results demonstrate the need to consider workload adaptive and thermal aware in designing future reconfigurable accelerator architecture. Offering a balance between performance, thermal stability, and energy efficiency, the presented framework offers an opportunity to make high-performance computation on edges to be sustainable.

Discussion

The conducted experiment indicates the benefits of combining thermal consciousness and workload adaptability with VLSI accelerator architectures that are used in edge-AI applications. The classical design of accelerator usually focuses on the performance metrics like throughput and latency and is not aware of the thermal implications of sustained computation. Nevertheless, in edge devices with weak cooling abilities, the overheating can have serious repercussions on the stability of the system and its longevity. The proposed architecture will solve this problem by deploying a scheduling strategy that will temporarily redistribute workloads based on the predicted module temperatures. Through constant checking and estimations of thermal conditions, the system guarantees that none of the processing unit emit a thermal hot spot. The improvement of the performance with the help of the dynamic reconfiguration of the pipeline with the dataflow is another meaningful study that was obtained. The architecture is not bound to allocate the hardware modules to specific tasks instead of dynamically allocating processing resources depending on the workload demand. This will allow making good use of the hardware resources available, particularly when heterogeneous loads are being run in parallel. In addition, synthetic workload generation is used to make the evaluation methodology reproducible and non-application specific datasets. This is necessary reproducibility in architectural design decisions in earlier hardware development phases.

Conclusion

This study proposed a thermal and work load aware reconfigurable VLSI based accelerator architecture to support high performance edge-based AI signal processing applications within severe power and thermal limits. The proposed architecture comprises of modular processing units, joined by a dynamically configurable dataflow network that enables the accelerator to fit the heterogeneous signal processing workloads. The proposed system allows the dynamic allocation of processing modules based on real-time workload requirements, unlike traditional fixed-resource conventional accelerator systems, which allocate fixed hardware resources to fixed tasks. This allows the accelerator to be used to run a wide range of edge-AI applications, including image processing, radar signal analysis, and audio feature extraction, and brings all these applications into a single hardware platform.

One of the contributions made by this work is the implementation of a thermal aware work load scheduling algorithm which keeps estimating the thermal conditions of processing modules and reassigns workloads to avoid localised overheating. The architecture can optimally balance the load of computations among modules by making use of temperature prediction in the scheduling process, and this way avoids thermal hotspots that otherwise may cause system reliability. Experiments of the simulation using synthetic signal-processing workloads indicate that the suggested architecture leads to a significant increase in the performance of the system and does not change the thermal characteristics.

The experimental statistics point out the reconfigurable accelerator would have about 32 percent higher processing throughput, 18 % reduced energy, and some 12°C decreased peak module temperature over the baseline static accelerator architectures. These demonstrate the potential benefits of bringing in workload adaptivity and thermal awareness into accelerator design in edge computing applications where cooling is a significant constraint and energy efficiency is an important factor.

In general, the proposed framework has offered a simulation-based approach to assessing architecture trade-offs in upcoming generation edge-AI hardware systems prior to their embodiment in hardware. The architecture provides a scaled solution whereby modular reconfigurable processing units can be combined with smart scheduling strategies to provide an architecture that can be adjusted to meet changing signal-processing workloads. Future studies will

include adaptive scaling of voltage and frequency, hardware-software power controls, and machine-learning-based timing and scheduling algorithms to achieve an even greater increase in energy efficiency and operational reliability in reconfigurable accelerator systems to edge-AI computing systems.

References

Bobda, C., Mbongue, J. M., Chow, P., Ewais, M., Tarafdar, N., Vega, J. C., ... & Tessier, R. (2022). The future of FPGA acceleration in datacenters and the cloud. *ACM Transactions on Reconfigurable Technology and Systems (TRETS)*, *15*(3), 1-42. https://doi.org/10.1145/3506713

Miliadis, P., Theodoropoulos, D., Pnevmatikatos, D. N., & Koziris, N. (2022, September). VenOS: A virtualization framework for multiple tenant accommodation on reconfigurable platforms. In *International Symposium on Applied Reconfigurable Computing* (pp. 181-195). Cham: Springer Nature Switzerland. https://doi.org/10.1007/978-3-031-19983-7_13

Rodríguez, A., Valverde, J., Portilla, J., Otero, A., Riesgo, T., & De la Torre, E. (2018). Fpga-based high-performance embedded systems for adaptive edge computing in cyber-physical systems: The artico3 framework. *Sensors*, *18*(6), 1877. https://doi.org/10.3390/s18061877

Reagen, B., Adolf, R., Shao, Y. S., Wei, G. Y., & Brooks, D. (2014, October). MachSuite: Benchmarks for accelerator design and customized architectures. In *2014 IEEE International Symposium on Workload Characterization (IISWC)* (pp. 110-119). IEEE. https://doi.org/10.1109/IISWC.2014.6983050

Atieh, A. T. (2021). The next generation cloud technologies: a review on distributed cloud, fog and edge computing and their opportunities and challenges. *ResearchBerg Review of Science and Technology*, *1*(1), 1-15.

Xu, C., Jiang, S., Luo, G., Sun, G., An, N., Huang, G., & Liu, X. (2020). The case for fpga-based edge computing. *IEEE Transactions on Mobile Computing*, *21*(7), 2610-2619. https://doi.org/10.1109/TMC.2020.3041781

Migali, A., Spagnolo, F., & Corsonello, P. (2022, June). Heterogeneous FPGA-based system for real-time drowsiness detection. In *2022 17th Conference on Ph. D Research in Microelectronics and Electronics (PRIME)* (pp. 169-172). IEEE. https://doi.org/10.1109/PRIME55000.2022.9816816

Abdullah, D. (2025). Event-Triggered Causal Learning Implementation for Real-Time Frequency Control on Embedded Energy Management Platforms. *Archives of Embedded and IoT Systems Engineering*, 18-25.

Capra, M., Peloso, R., Masera, G., Ruo Roch, M., & Martina, M. (2019). Edge computing: A survey on the hardware requirements in the internet of things world. *Future Internet*, *11*(4), 100. https://doi.org/10.3390/fi11040100

Kavitha, M. (2025). Energy-Efficient Edge-AI Accelerator Design Using Reconfigurable FPGA-Based VLSI Architecture. *Journal of VLSI and Embedded System Design*, *1*(1), 26-33.

Liu, L., Zhu, J., Li, Z., Lu, Y., Deng, Y., Han, J., ... & Wei, S. (2019). A survey of coarse-grained reconfigurable architecture and design: Taxonomy, challenges, and applications. *ACM Computing Surveys (CSUR)*, *52*(6), 1-39. https://doi.org/10.1145/3357375

Lee, K. J. (2021). Architecture of neural processing unit for deep neural networks. In *Advances in computers* (Vol. 122, pp. 217-245). Elsevier. https://doi.org/10.1016/bs.adcom.2020.11.001

Novac, P. E., Boukli Hacene, G., Pegatoquet, A., Miramond, B., & Gripon, V. (2021). Quantization and deployment of deep neural networks on microcontrollers. *Sensors*, *21*(9), 2984. https://doi.org/10.3390/s21092984

Reginald, P. J. (2025). Reconfigurable Embedded Control Architectures for Cooperative Learning-Based Robust Electromechanical Systems. *Archives of Embedded and IoT Systems Engineering*, *2*(3), 1-9.

Xia, Q., Ye, W., Tao, Z., Wu, J., & Li, Q. (2021). A survey of federated learning for edge computing: Research problems and solutions. *High-Confidence Computing*, *1*(1), 100008. https://doi.org/10.1016/j.hcc.2021.100008

Cui, L., Yang, S., Chen, F., Ming, Z., Lu, N., & Qin, J. (2018). A survey on application of machine learning for Internet of Things. *International Journal of Machine Learning and Cybernetics*, *9*(8), 1399-1417. https://doi.org/10.1007/s13042-018-0834-5

Rahim, R. (2025). Secure and Energy-Optimized VLSI Architecture for Edge-Enabled Embedded Systems. *Journal of VLSI and Embedded System Design*, 41-48.

Kum, S., Oh, S., Yeom, J., & Moon, J. (2022). Optimization of edge resources for deep learning application with batch and model management. *Sensors*, *22*(17), 6717. https://doi.org/10.3390/s22176717

Mishra, N. (2025). Scalable Graph-Centric Data Engineering for Energy-Harvesting Intelligence in 6G IoT Networks. *Journal of Scalable Data Engineering and Intelligent Computing*, *2*(2), 1-8.

Dineshkumar, P. (2024). AI-Based Predictive Maintenance in Industrial Robotics. *SECITS Journal of Scalable Distributed Computing and Pipeline Automation*, *1*(1), 32-38.

Tandi, M. R. (2024). Secure Peer-Assisted Communication Protocols for Distributed E-Learning Systems. *Transactions on Secure Communication Networks and Protocol Engineering*, 40-50.

Sindhu, S. (2025). Design and Implementation of a Low-Power Reconfigurable Antenna for 5G Mobile Communication Systems. *Journal of Reconfigurable Hardware Architectures and Embedded Systems*, *2*(2), 32-41.

Rahman, F. (2025). Event-Triggered Learning Control for Adaptive Embedded Networked Systems. *Journal of Reconfigurable Hardware Architectures and Embedded Systems*, *2*(3). 35-40.

Prashanth, R. (2024). Intelligent Cyber Threat Detection Using NLP and Semantic Knowledge Graphs. *Journal of Wireless Intelligence and Spectrum Engineering*, *1*(1), 33-39. https://doi.org/10.17051/JWISE/01.01.05

Suresh kumar, A. (2024). A Federated Learning Framework for Secure IoT Data Analytics in Smart Home Environments. *National Journal of Ubiquitous Computing and Intelligent Environments, 1*(1), 21–30.

Hugh, Q. (2024). Blockchain-Based Data Integrity Framework for Secure Cloud Storage Systems. *Transactions on Internet Security, Cloud Services, and Distributed Applications*, *1*(1), 8-14. https://doi.org/10.17051/TICDA/01.01.02

Srikanth Reddy Keshireddy. (2025). AI-Driven Anomaly Detection and Behavior Analytics in Heterogeneous IoT Ecosystems. *Progress in Electronics and Communication Engineering*, *2*(2), 47-53. https://doi.org/10.31838/c37qct97

Chia-Hui, C., Ching-Yu, S., Fen, S., & Ju, Y. (2025). Designing scalable IoT architectures for smart cities: Challenges and solutions. *Journal of Wireless Sensor Networks and IoT*, *2*(1), 42-49. https://doi.org/10.31838/WSNIOT/02.01.05

Arun Prasath, C. (2024). Optimization of FPGA Architectures for Real-Time Signal Processing in Medical Devices. *Journal of Integrated VLSI, Embedded and Computing Technologies*, *1*(1), 11-15. https://doi.org/10.31838/JIVCT/01.01.03

De Mindonça, F, & Smith, O.L.M. (2025). Self-Supervised Audio Representation Learning for Robust Speaker Verification. *National Journal of Speech and Audio Signal Processing*, *1*(4), 26-33. https://doi.org/10.17051/NJSAP/01.04.04

Velliangiri, A. (2025). Energy-efficient building design using bio-inspired materials and machine learning optimization. *Journal of Smart Infrastructure and Environmental Sustainability*, *2*(1), 21-30. https://doi.org/10.17051/JSIES/02.01.03

Brinda, B. M. (2025). Smart Aquaculture Monitoring and Control Using AI-Driven Water Quality and Fish Health Analytics. *National Journal of Smart Fisheries and Aquaculture Innovation*, *3*(2), 9-18.

Prabhakar, C. P., & Tamrakar, G. (2025). Advanced Numerical Techniques for Solving High-Dimensional Integral Equations in Environmental Engineering Applications. *Journal of Applied Mathematical Models in Engineering*, *1*(4), 9-16. https://doi.org/10.17051/JAMME/01.04.02

Dineshkumar, P. (2025). Managing Cultural Authenticity in Tourism Destinations: Impacts on Tourist Satisfaction and Revisit Intention. *Journal of Tourism, Culture, and Management Studies*, *2*(3), 1-9.

Saranya, N. (2025). Integrating Total Quality Management and Innovation Strategy: An Empirical Study of Business Excellence Performance. *National Journal of Quality, Innovation, and Business Excellence*, *2*(3), 9-16.

Jun, L., & Kim, L. (2025). Quantum Computing for Precision Medicine: Current Applications and Future Directions. *Frontiers in Life Sciences Research*, *1*(4), 8-14.