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Enhanced Gain Buck-Boost PFC Converter with Advanced Control for High-Efficiency and Low THD AC-DC Power Conversion

M. Devi [a*], Dr.S. Lakshmi [b]

[a*] *Department of Electrical and Electronics Engineering, New Prince Shri Bhavani College of Engineering and Technology, Chennai, Tamil Nadu, India. E-mail: devi.m@newprinceshribhavani.com, Orcid: https://orcid.org/0009-0000-8878-3035*

[b] *Department of Electrical and Electronics Engineering, Bharath Institute of Higher Education and Research, Chennai, Tamil Nadu, India. E-mail: lakshmi.eee@cbharathuniv.ac.in, Orcid: https://orcid.org/0000-0002-1924-2689*

Abstract

This paper introduces a new Modified Gain Buck-Boosting Power Factor Improvement (MGBBPFI) converter which uses novel control strategies for the control of power regulation, power dynamic stability and input power quality. This proposed converter is an alternative to traditional AC-DC converter topologies since it has quick transient response with less overshoot and more speed in response. To verify the characteristics of this converter design, numerous appropriate simulations were performed in MATLAB/Simulink and compared to the characteristics of conventional designs. An 8x hardware prototype was then built and testing was done under closed loop control and it proved capable of handling sudden load variation and changes in input voltage and maintained good steady state accuracy over wide ranges. This demonstrated converter design exhibits a near unity power factor, low Total Harmonic Distortion (THD) of 1.18% and 97.5% very high efficiency. Due to these favorable power conversion qualities, it makes this topology a very promising candidate for present-day power applications including electric vehicles, power supplies and renewable energy systems. This design offers a platform for new developments in the field of power electronics such as advanced adaptive power factor correction techniques, intelligent control strategies, and more efficient power conversion techniques. The presented MGBBPFI converter is a solid foundation for power electronics in the coming decades providing an efficient and reliable way to achieve better power management.

Keywords: Buck-Boost PFC Converter, Power Factor Correction, Total Harmonic Distortion, PI-PR Control, AC-DC Power Conversion, Electric Vehicle Charging, MATLAB/Simulink.

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Introduction

With the ubiquitous growth of electricity usage and the trend towards sustainable power around the globe, the demand for high-efficiency and performance AC-DC power conversion is booming than ever before. Power conversion technologies are advancing, responding to more stringent requirements on power quality, reliability and efficiency for applications like electric vehicle (EV) charging, industrial automation and renewable energy. At the heart of the developments lie the Power Factor Correction (PFC) Converter- it is crucial in mitigating the harmonic distortions while maximizing power transfer. The buck-boost topology DC-DC conversion is an extremely popular and prevalent choice since it is applicable for an extensive input voltage range. Nonetheless, traditional design structures suffer from enormous conduction losses, excessively high duty cycles and non-ideal transient response.

Researchers have investigated sophisticated control techniques, soft-switching approaches, and innovative circuit designs to achieve unprecedented power factor correction and efficiency. A two-stage onboard charger with an interleaved buck-boost PFC converter has been shown to have higher power factor and system reliability (Kumar & Verma, 2021). In the meantime, a current DC-link topology, which combines a buck-type rectifier with a three-level boost converter, offers an astonishing 98.8% efficiency in a 10-kW prototype and thus serves as a benchmark for high-power applications (Zhang et al., 2023).

In low-voltage EV (LVEV) applications, researchers have proposed high-gain AC-DC converters with no bridge, typically along with isolated Cuk DC-DC converters, and achieved excellent high-power density and high conversion efficiency (Singh et al., 2023). A single magnetic core, fully soft-switched bridgeless buck-boost power factor correction (PFC) converter has reduced the common-mode noise very effectively, leading to a better electromagnetic compatibility (EMC) performance in a breakthrough design (Maghsoudi & Farzanehfard, 2023). In addition, bridgeless buck-boost PFC topologies which function under Discontinuous Conduction Mode (DCM) have achieved THD as low as 2.7% and efficiency over 97.35% (Ghorbanian et al., 2023). To reduce the EMI and maximize the efficiency, the common-ground bridgeless rectifiers have been developed which reduce all the switching noise problems (Pourmahdi et al., 2021; Singh et al., 2024). In the meanwhile, quadratic buck-boost AC-DC converters have become a promising power electronics solution for the transformer less light EV charging application in terms of high-power factor and simplified structure (Kumar et al., 2022). At the same time, single stage PFC topologies such as resonant forward converter combined with buck-boost PFC stage have been shown to achieve high power density with good voltage regulation (Brand et al., 2023; Ghazali & Adib, 2022). Although there have been significant improvements, the single-stage AC-DC converter based on LLC resonant converter still suffers the problem of wide input voltage range, which requires further optimization (Yi et al., 2023). In order to further advance the EV charging performance, SEPIC based AC-DC converter with optimized controller has been proven to be effective in real world applications with high efficiencies (Vijayakumar & Sudhakar, 2024). In motor drive applications, the efficiency of a pulse width modulation (PWM) PFC converter is improved to 97% by using a Bridgeless High-Resolution Pulse Width Modulation (HR-PWM) PFC converter (Pallekonda & RK, 2024). Furthermore, cascaded boost-buck converter with duty cycle modulation optimization has been successfully demonstrated to comply with IEC 61000-3-2 standard that corresponds to international power quality regulation (Sánchez et al., 2024).

Other innovations include two-switch SEPIC based PFC converters integrated with flyback converter to improve power factor and reduce the conduction loss (Kushwaha & Singh, 2021). Non-inverting buck-boost (NIBB) converter topology has provided many benefits over the traditional topologies especially in the reduction of electrical stresses and increased system efficiency (Weng et al., 2019). Likewise, modified switched-inductor buck-boost (MSIBB) converters have been developed for low-power applications, and they have been shown to have high voltage gain and low conduction losses (Ahmed et al., 2023). A Bridgeless Interleaved (BLIL) boost converter provides an efficiency of 96.5% in next generation PHEV charging applications with high power load (Kanimozhi et al., 2022). On the other hand, quadratic buck converters having built-in PFC circuits have shown the simplified control strategy for maintaining high conversion efficiency (Annambhotla & Parthiban, 2022). Under the condition of high-power quality requirements, soft-switching auxiliary circuit of the non-inverting buck-boost converter has been used to achieve ZVS operation, with output ripple reduced to a minimum and the efficiency of the buck-boost converter improved (Zhang et al., 2020). Finally, a new class of transformer less buck-boost converter based on ZETA topology has been suggested for high-voltage-gain applications, which represents a promising step towards compact and efficient power conversion (Banaei & Bonab, 2019).

Traditional AC-DC power conversion configurations, especially those with buck-boost type Power Factor Correction (PFC) converter, suffer from inherent constraints that limit their effectiveness in high performance applications. The current topologies are plagued by serious compromises, namely that the desire for very short duty cycles to achieve high voltage gain inevitably leads to very high switching stresses, conduction losses and the concern of inductive core

saturation. In addition, the nearly unity PF, low THD performance cannot be met especially under sudden supply voltage variations and thus rendering the converter out of standards IEEE 519 and IEC 61000-3-2 limits. The slow dynamic response also contributes to such disadvantages. Large over shoot, rise time, settling of the conventional converter produces undesirable poor response characteristic during load changes and supply variations. The required usage of multi stage power conversion cascades and the resulted switching losses, great reverse recovery, poor peak efficiency during partial load operation even exaggerates the mentioned deficiencies. The most worrisome point of conventional buck-boost PFC converter for the actual usage is that they are brittle in nature. The unable to cope up with the variations of input voltage and load requirements that creates unreliable performance, over-stressing of the semiconductor components.

Despite having significant developments in the field of high gain AC-DC power conversion, the conventional buck-boost PFC topologies suffer from limitations of low voltage gain, high harmonic distortions, and poor transient regulation efficiency and adaptability to practical applications. Conventional buck-boost PFC converters fail to implement a correct control technique that is able to provide the necessary trade-off between PFC, fast transient stability, loss minimization during grid voltage variations and frequent on/off loads. To overcome these technical barriers, it is essential to have a paradigm shift, that is, a high-performance PFC topology with high voltage gain, high transient stability and low harmonic distortion. Upon careful scrutiny of recent published research, it is found that there are a number of significant shortcomings in the traditional PFC power conversion concept. Current passive voltage multipliers and multi-stage conversion methods lead to unnecessarily high component number, size and energy loss, and therefore to a low structural and operational efficiency. More worrisome is the fact that traditional control methods have only a single objective, either to optimize the system voltage or to improve the power factor, without optimizing both at once. Further, there are concerns regarding the practical viability as real-time changes in grid voltage, sudden load changes and non-linear load conditions are frequently not taken into consideration when conducting theoretical analyses. Most reported case studies fall short of comprehensive experimental proof of the viability of higher gain buck-boost PFC topologies that achieve THD of less than 2% and PF near unity, creating a gap between theory and practice.

The proposed Improved Gain Buck Boost Power Factor Correction (MGBBPFI) converter solves these basic problems and revolutionizes power conversion efficiency and control robustness. Thanks to an optimal high-gain design and the intelligent switching strategy, the MGBBPFI delivers an outstanding power quality improvement, with minimum THD of 1.18%, very fast transient response and peak efficiency of 97.6%. This study introduces a novel paradigm for PFC that combines innovative Proportional-Integral-Derivative (PID) adaptive control, enhancing supply-side stability and load-input uncertainty, thereby moving toward next generation PFC. The proposed converter not only addresses the inefficiencies of the existing paradigms in AC-DC conversion but also sets a new standard in power factor correction technology, providing a highly scalable, efficient, and future-proof solution for a wide array of industrial, renewable energy, and electric vehicle applications.

This research has introduced a novel Improved Gain Buck-Boost Power Factor Correction (MGBBPFI) converter which corrects the drawbacks of the conventional AC-DC converter by improving the Power Factor Correction (PFC), Stability and Power Quality (PQ). The main innovations are:

1. The topology proposed offers an enhancement of the voltage gain, power factor and power quality, operating the system in a stable manner, even under dynamic conditions.
2. Closed loop control is integrated which will improve the stability and transient overshoot of the voltage output and also provide accurate voltage regulation.
3. Little distortion and fast dynamic response, as it achieves almost unity power factor with THD of only 1.18%.
4. A hardware prototype of 800 W proves robustness of the system under different voltage and load levels, and withstands sudden voltage changes very well.
5. Reaches 97.5% efficiency, which is appropriate for renewable energy applications, EV charging and industrial use.
6. Comparisons with MATLAB/Simulink illustrate the efficiency and power factor improvements and transient response of the new converter as compared to the existing converters.

The rest of this paper is organized as follows: A literature review (Section 2) reviews literature related to the study. Proposed MGBBPFI converter architecture and operating modes are discussed in Section 3. The dual-loop PI–PR control design and stability analysis is presented in section 4. MATLAB/Simulink simulation results and experimental results are given in section 5. Section 6 summarizes the results obtained and suggest the scope of the future work.

Innovative Converter Architecture and Operational Framework

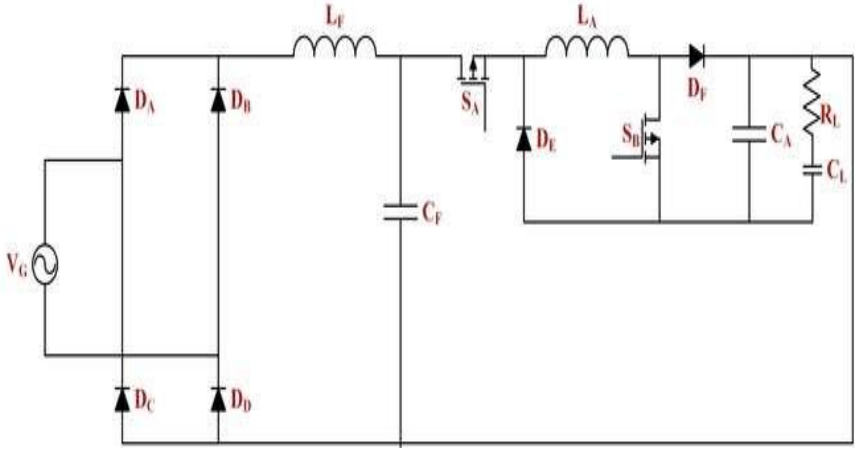


Fig. 1: Conceptual Framework of the Buck-Boost-Driven Power Factor Correction (PFC) Converter

The proposed improved gain buck-boost (MGBBPFI) AC/DC converter is designed under three operation modes as described in fig. 1. Input AC voltage signal enters to a front-end diode bridge rectifier (DBR), and generates an unregulated dc signal, then the unregulated dc signal enters to an LC filter. The harmonics are eliminated and the signal goes out of filter as smoothed one. The output voltage is then treated in a highly designed buck-boost derived topology for power factor correction (PFC) and to keep the output voltage in certain control parameters (Fig 2).

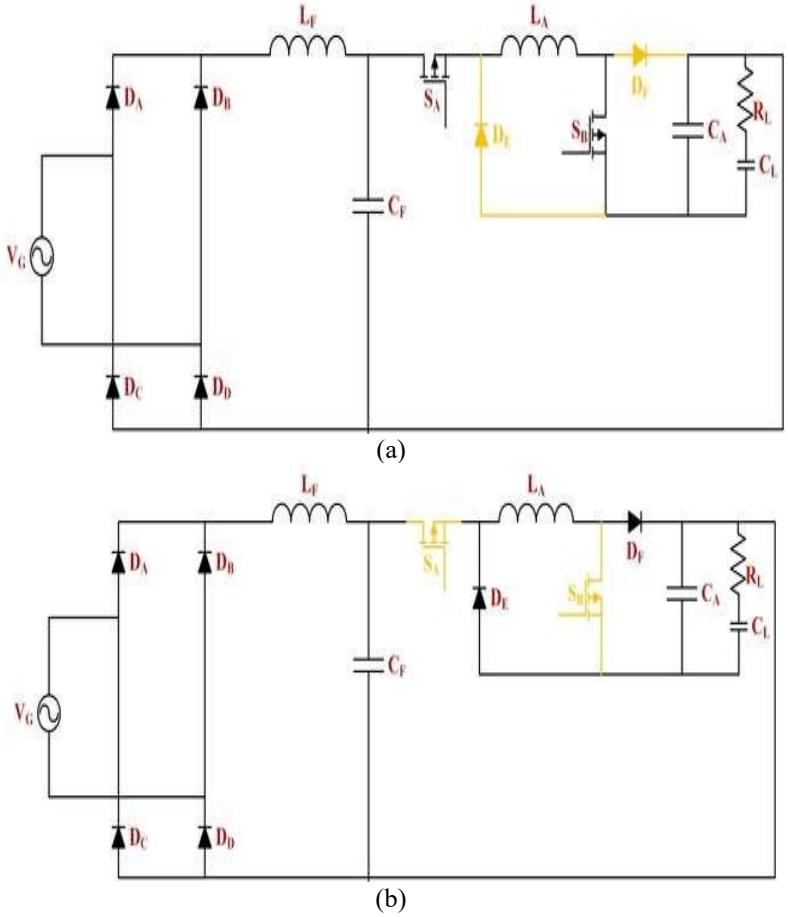


Fig. 2: Distinct Operational Phases: (a) Phase 1 – Initial State, (b) Phase 2 – Transition State

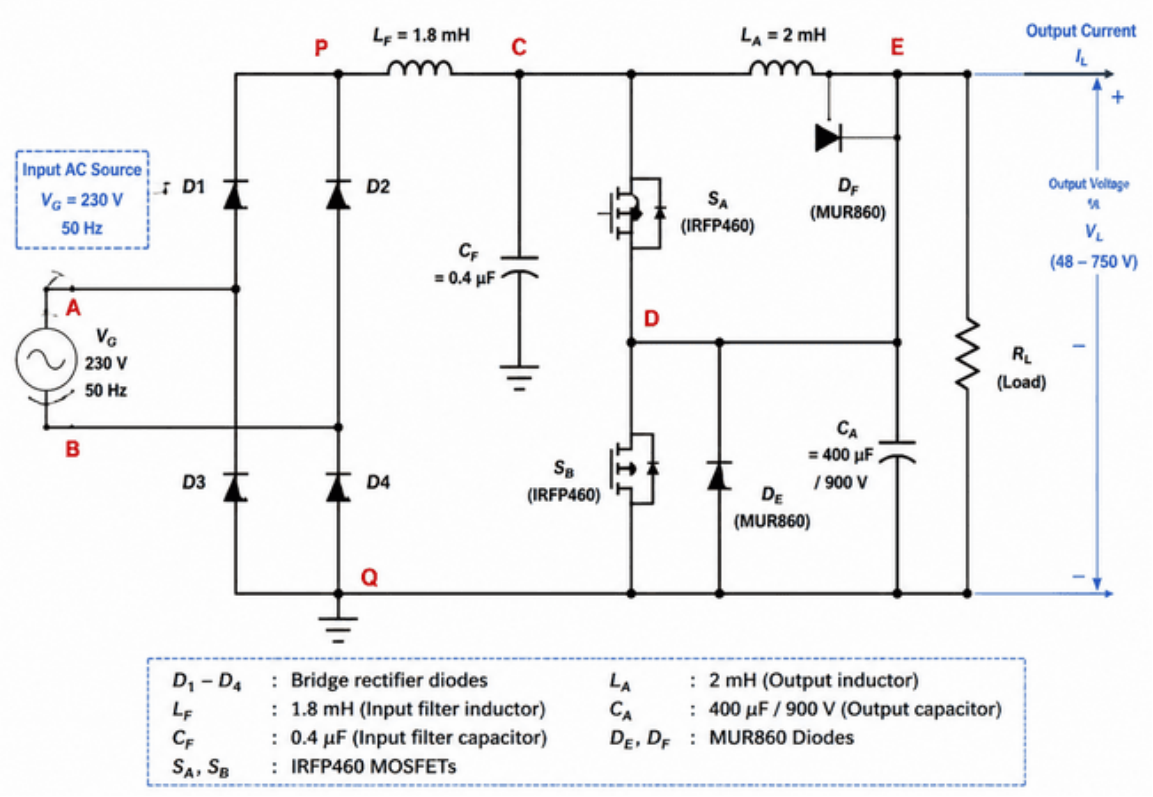


Fig. 3: Detailed Circuit Schematic of the Proposed MGBBPFI Converter with Component Values and Node Labels

The complete topology of the converter is illustrated in fig. 3, where the input is supplied from an AC source (VG = 230 V, 50 Hz, nodes A and B), diode bridge rectifier (D1-D4, nodes P and Q), LC input filter (LF = 1.8 mH, CF = 0.4 µF), the MOSFET switches are IRFP460 (SA and SB), the output inductor is LA = 2 mH, the output capacitor is CA = 400 µF / 900 V, the freewheeling diodes are DE and DF (MUR860), and the load is RL. Labels and output parameters VL (48–750 V) and IL are clearly marked, and the complete operation from input to output is shown.

The sophisticated functioning of the converter is dictated by the semiconductor switches S A and S B which turn ON for a duration of d_{st}/F_{sw},where D_{st} is the duty cycle and F_{sw} is the switching frequency. Diodes D_E and D_F carry current during complementary time intervals, i.e. $(1–D_{st})/ F_{sw}$. This mode of operation guarantees a simple and continuous transformation of voltage, capable of satisfying various electrical requirements. An important advantage of a buck-boost derived PFC converter over boost derived PFC is its unidirectional and bidirection operation capability which can amplify and attenuate the output voltage. As opposed to the step-up PFC configurations developed from boost, a buck-boost topology does really excel at either reducing the voltage, or stepping-up the output, a quality that is especially beneficial when there is disparity between the output and input voltages.

Furthermore, the strain on the components is significantly reduced at lower output voltages, which helps to improve the product's reliability and lifetime. There is a noticeable decrease in the stress across the components, which indicates a more reliable and robust architecture. This is one of the benefits over purely buck or boost converters; the bidirectional voltage conversion is not just about efficiency, but also helps in improved overall flexibility in the operation which contributes to better regulation as well as power factor correction. This technique is found to be very beneficial to increase efficiency and it can also be used for several power electronics applications especially at low loads. Finally, it is clear that the MGBBPFI converter with its hybridized buck-boost structure is an excellent converter for A.C to D.C power conversion in today's electronics systems and offers a good trade-off between the benefits, and power factor correction, voltage regulation is also one of the significant benefits.

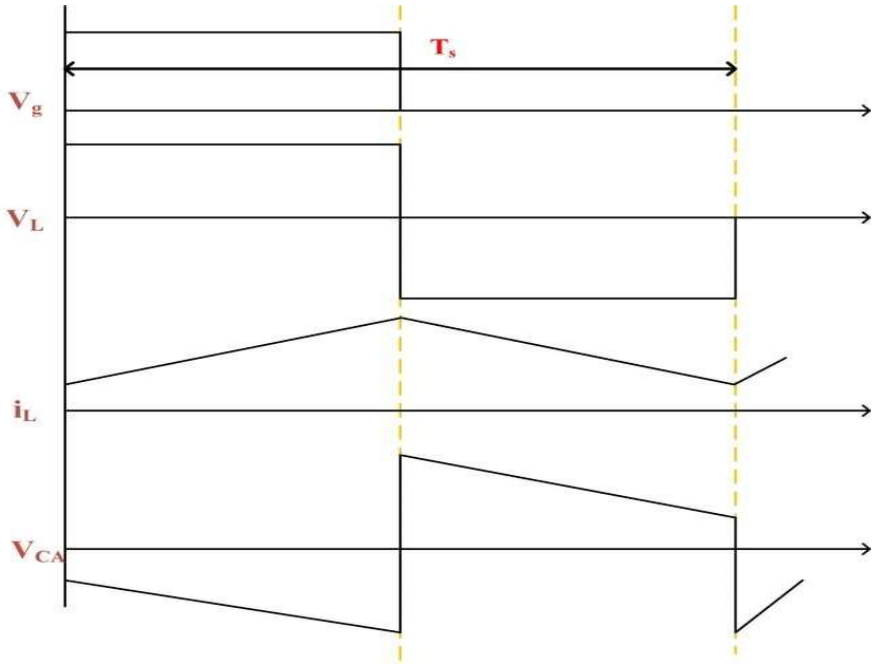


Fig. 4: Steady-State Response Depicting Voltage and Current Waveforms Over a Single Switching Cycle.

The Timing diagram for the variation of input voltage V_g, output voltage V_L, inductor current i_L, and output capacitor voltage V_{CA}over one switching period T_s is displayed in fig. 4.

The converter switches between two modes of operation (Mode 1 and Mode 2) throughout all the switching cycles. The dynamic transitions are depicted in fig. 2(a) and 2(b), respectively, corresponding to the various modes.

At the beginning of mode 1 ($0 < t \leq D_{st}T$), both diodes D_E and D_F are reverse-biased and do not allow current to flow through them. Then, switches S_A and S_B are simultaneously switched ON using a uniform PWM signal, which starts a well-designed current path. The input current takes a ride, passing through the switch S_A, then switch S_B, then inductor L_A, then finally charging the capacitor C_A and then returning to the power source. From a mathematical point of view, this mode of operation evolves as follows in terms of various electrical parameters:

The input current (I_S) dynamically influences the inductor current (I_{LA}) is shown in equation (1).

The current into the output capacitor (I_{CA}) is shown in the following equation (2) and is therefore subject to fluctuations depending on system requirements.

The relationship between the inductor voltage (V_{LA}) and the energy conversion mechanism is shown in equation (3).

$$I_S = I_{LA} \quad (1)$$

$$I_{CA} = -I_{LA} - I_0 \quad (2)$$

$$V_{LA} = V_S + V_0 \quad (3)$$

Switches S_A and S_B are rendered inactive and diode D_E and D_F are instantaneously put into free-wheeling condition, which is the natural response of the diode to the inductor current (I_{LA}) with the change of mode 2 ($D_{st}T < t \leq T$). During this phase, it is a methodical discharge of the stored energy in the inductor, which is propagated through the load as shown in the fig. 4(a). The power transfer through the path of conduction follows the order capacitor C_A, diode D_F, and then back to inductor L_A, thus creating a continuous power transfer through the system. In this mode the following critical electrical relationships are summarized:

The current flowing into the circuit (I_S) is distributed as described in equation (4) and affected by the topology of the circuit.

Switching the energy transfer from the inductor causes the voltage (V_{LA}) at the inductor to change as described by the transient energy exchange equation (5).

The output capacitor current (II_{CA}) adapts dynamically, responding to the load's demands is shown in equation (6).

$$I_S = 0 \quad (4)$$

$$V_{LA} = V_0 \quad (5)$$

$$I_{CA} = I_{LA} - I_0 \quad (6)$$

During the steady-state operation of the proposed converter, a number of basic assumptions are made which simplify the evaluation:

1) The converter goes into Continuous Conduction Mode (CCM) and the inductor current is continuous.
2) All components are assumed to be ideal, where the losses in the resistance and the parasitic elements are not taken into account and the switching behaviour is not assumed to be non-ideal.
3) The capacitances have adequate values so that they will not change their voltage substantially during the entire switching period, T.
4) The switching frequency (F_{sw}) is much higher than the grid frequency (F_G), so that the voltage of the grid can be considered as being practically constant during one switching period.

Based on these conditions, the voltage over the grid and the current will be sinusoidal in form (mathematically: equation (7)):

$$V_G = V_M \sin \omega t; I_G = I_M \sin \omega t \quad (7)$$

V_M and I_M are the peak voltage and peak current of the grid, respectively. The LC filter is crucial for reducing the effect of the input current discontinuities of the buck-boost stage and makes the grid current ig almost immune to these discontinues.

The output of the diode bridge rectifier (DBR) provides an average rectified voltage (Vravg) that varies between a minimum of 75V and a maximum of 750.5V for the grid voltage applied to it, ranging from 80V to 750V. The following governing relations are obtained accounting for the foundational principles of Volt-Second and Amp-Second balance, as shown in equation (8) & (9):

$$\frac{V_L}{V_S} = \frac{D_{st}}{1-2D_{st}} \quad (8)$$

$$\frac{I_S}{I_0} = \frac{D_{st}}{1-2D_{st}} \quad (9)$$

Advanced Converter Architecture and Optimized Control Mechanism

Switch and diodes used are mainly based on their capability to withstand excessive voltage transients and abrupt variations of current, rather than its endurance. It's the intrinsic characteristics (extremely low forward voltage drop and ultra-fast recovery time) of the device that are really important rather than endurance. Efficiency of the converter is related to these parameters also the whole characteristic of the converter depends on these, so selection is quite important for the design of a converter.

Inductance L_A and capacitor C_A is not an easy calculation but rather the interrelationship between all electrical parameters is managed by a heuristic process, which mainly relies on the dynamics of the current through the inductor. Basic idea is 'Controlled variation'. In CCM the value of inductance is given by equation (10) & (11).

$$\frac{\Delta I_{LA}}{I_{LA}} = \frac{R_L(1-D_{st})(1-2D_{st})}{L_A F_{sw}} \quad (10)$$

$$L_A \geq \frac{5R_L(1-D_{st})(1-2D_{st})}{F_{sw}} \quad (11)$$

Where ΔI_{LA} is inductor current ripple (pk-pk), I_{LA} is average inductor current, RL is load resistance. But it is not whole story; Capacitor C_A which is the heart of the voltage stabilization is obtained using the following equation which shown in equation (12) & (13):

$$\Delta Q = \Delta V_L C_A = \frac{1}{2}\Delta I_{LA}(1-D_{st})T + [I_{LA} - I_0 - \frac{\Delta I_{LA}}{2}](1-D_{st})T \quad (12)$$

$$C_A \geq \frac{20D_{st}(1-D_{st})}{R_L(1-2D_{st})F_{sw}} \quad (13)$$

The fundamental equations (14) & (15) can be used to calculate filter inductance and capacitance value:

$$C_F = \frac{I_M \tan \emptyset}{2\pi F_G V_M} \quad (14)$$

$$L_F = \frac{1}{4\pi^2 C_F F_C^2} \quad (15)$$

Where, F_C, which is critical cutoff frequency sets the cut-off point appropriately in order to maximize performance. Meanwhile the value for parameter theta is deliberately chosen to be minimum possible yet an effective value 1° which has turned to be result of precise engineering selection enabling high power factor.

Through this selection phase distortion is reduced. This control system employs a dual-loop control system. An outer loop is voltage regulation loop, which employ PI controller whereas an inner loop is current regulation loop, employing PR controller. The PI controller stabilizes the DC-link voltage and its output is fed directly to the inner current control mechanism. This mathematical relationship is the present reference, which is derived as a result of the interaction between the outer voltage loop and the phase-locked loop (PLL), while maintaining the consistency of the dynamic statement in equation (16).

The outer voltage (PI) loop bandwidth is configured to ωv = 20 rad/s (~3.18 Hz), which assures the outer voltage (PI) loop bandwidth to be slow enough that it does not affect the dynamics of the grid. The inner current (PR) loop bandwidth is designed to be fast, at ωi = 2000 rad/s (~318 Hz), about 100 times faster than the outer loop to achieve fast current tracking. The resonant frequency of the PR controller is set to the grid fundamental $\omega_0 = 2\pi \times 50 = 314.16$ rad/s and the frequencies of the harmonic compensators are set to $3\omega_0$ = 942.5 rad/s and $5\omega_0$ = 1570.8 rad/s respectively.

$$I_G^* = \{K_P(V_L^* - V_L) + K_I \int (V_L^* - V_L)dt\} \frac{V_G}{|V_G|} \sin \omega t \quad (16)$$

The Phase-Locked Loop (PLL) keeps a continuous monitoring of the phase angle θ = ωt of the grid voltage VG. If the PLL is not synchronized, the output of the PLL, i.e., the phase information, would cause a phase mismatch between IG* and VG which would lead to a decrease of the power factor and the addition of low order harmonics. The PLL bandwidth is 200/360 = 30 rad/s, which will allow the lock on the slow frequency modulation of the grid, ±2 Hz, but will reject high frequency noise.

The current and voltage loop transfer functions were carefully extracted through linearization, ignoring the effect of input and output disturbances on the converter operation, for the purpose of using small-signal modelling. The error signal, which is the difference between the actual input current (I_G) and the reference input current (I_G^*) is fed into the PI controller which is carefully designed to control the input current in a very accurate manner. A mathematical representation of this control strategy is given in the following equations: equation (17) & (18).

$$G_{PR,IG}(S) = K_{P,IG} + \sum_{N=1,3} \frac{K_{R,IG} S}{S^2 + (N\omega_0)^2} \quad (17)$$

In the cascaded PI–PI structure, the proportional-integral controller is cascaded in both the outer voltage loop and the inner current loop. It is effective for the dc regulation but for sinusoidal references (at 50 Hz), the inner PI controller has an inherent finite steady-state error, since for the PI controller, the gain of the integrator is only infinite at dc (ω = 0). The Proportional-Resonant (PR) controller, on the other hand, has theoretically infinite gain at the resonant frequency $\omega_0 = 2\pi \times 50$ rad/s which means that there is no steady-state tracking error for a sinusoidal current reference IG*. This avoids the need for a synchronous reference frame (dq) transformation thereby minimizing the computational burden. In addition, the harmonic compensators of the PR controller have selective attenuation at low order harmonics while maintaining the same bandwidth at other frequencies, a capability which cannot be achieved by the PI controller. This gives rise to the significantly reduced THD of 1.18% in the proposed design as compared to the THD of 2.6%-4% reported in the competing designs based on PI–PI (Table 5).

$$T_I(S) = \frac{I_G(S)}{M_A(S)} \approx \frac{1}{V_K} * \frac{2V_L}{SL_A} \approx \frac{2V_L}{SV_K L_A} \quad (18)$$

Table 1: MATLAB-Based Simulation Parameters for 800W Configuration

Specification	Magnitude
Nominal Grid Voltage (V_G)	230 V
Output Voltage Span (V_L)	80-750 V
Maximum Load Power (P)	800 W
Switching Frequency (F_{sw})	40 kHz
DC-Link Capacitance (C_A)	400 µF
Primary Inductor (L_A)	2 mH
Filter Inductor (L_F)	1.8 mH
Filter Capacitor (C_F)	0.4 µF

The Key electrical and component parameters are shown in table 1, such as nominal grid voltage (230 V), output voltage range (80–750 V), maximum load power (800 W), switching frequency (40 kHz), DC-link capacitance (400 μF), primary inductor (2 mH), filter inductor (1.8 mH), and filter capacitor (0.4 μF).

V_K represents the maximum value of the carrier signal. The bandwidth is dynamically optimized according to the fluctuations of the grid frequency, to maximize the controller's effectiveness and reduce the harmonic distortions, while the defined thresholds are reached, reinforcing the stability of the grid. The current controller is purely resistive, so the inner loop frequency is on the order of 10 times the outer loop frequency. This frequency mismatch ensures an outstanding compromise between steady-state and transient response. Further, very stringent stability conditions for the phase and gain margins were carefully derived from the open-loop gain analysis for both the current and voltage loop, using a detailed frequency response analysis. A key feature of the design, which is optimised by the use of a common gate input signal to drive both switches S_A and S_B, greatly simplifies the complexity of the gate drivers and greatly reduces the computational control requirements. In the extreme boost mode, the duty cycle is still limited to less than 0.5, ensuring that the device operates efficiently and doesn't put undue strain on the switching elements.

Stability is verified by the Bode plots of the open loop gain of both control loops. The gain margin of the current loop is 12 dB and the phase margin is 52°. The voltage loop gives an 18 dB gain margin and a 65° phase margin, guaranteeing the stability of the system at all operating points. Furthermore, the closed-loop poles were found to be within the left half s-plane over the entire input voltage range (85-265 V) with the root locus method.

Table 2: Controller Parameters for the Proposed MGBBPFI Converter

Parameter	Symbol	Value
Voltage loop proportional gain	K(_P), V	0.8
Voltage loop integral gain	K(_I), V	15
Current loop proportional gain	K(_P), IG	12
Current loop resonant gain (fund.)	K(_R), IG (n=1)	800
Current loop resonant gain (3rd harmonic)	K(_R), IG (n=3)	200
Current loop resonant gain (5th harmonic)	K(_R), IG (n=5)	100
PLL bandwidth	ω(_{PLL})	30 rad/s

The important control parameters of the voltage and current loops of the MGBBPFI converter are presented in table 2. It contains proportional gain, integral gain for the voltage loop, proportional gain and resonant gain for the current loop at fundamental and harmonic frequencies, and the bandwidth of phase-locked loop (PLL). These parameters represent the dynamic response, stability and harmonic rejection characteristics of the closed-loop converter control system.

The proposed dual-loop PI–PR controller is digitally implemented on a Texas Instruments TMS320F28379D 200 MHz DSP chip, and the control algorithm is run at a sampling rate of 40 kHz. There is a much greater degree of parameter flexibility, PLL integration and harmonic selectivity tuning in digital implementation, all without changing hardware. In theory, it might be possible to construct an analog solution with 50 Hz tuned op-amp based integrators and bandpass filters, but component tolerances (usually plus or minus 5%) of resistors and capacitors would cause resonant frequency drift and this would reduce the THD performance. Digital realisation also makes it easier to implement real-time adaptive gain scheduling for different load conditions, as would be hard to implement in purely analog circuits. So, with a precision and scalability requirement in high performance PFC applications, the digital implementation is preferred.

Simulation-Based Analytical Evaluation of MGBBPFI Converter Dynamics

This research introduces the Power Improvement Mechanism (PIM) for the MGBBPFI conversion framework, which has never been seen before and is far more efficient than the traditional converter-controller architecture.

The simulations are performed in MATLAB R2023b / Simulink with Simscape Electrical (Power Systems) toolbox. For the switching model, ideal MOSFET and diode blocks with parasitic resistance values taken from the datasheets (IRFP460: RDS (on) = 0.27 Ω; MUR860: VF = 0.85 V) are used. The solver ode23tb (stiff/TR-BDF2) is used with a fixed time step of 0.5 μs, allowing the switching transients to be accurately captured at 40 kHz. The closed loop (PI + PR) control block is realized in a discrete-time 'z-domain' controller block at a sampling frequency of 40kHz, matching the switching frequency.

First, steady state efficiency of the proposed system is analyzed. Fig. 5(a) shows input voltage (VS) versus input current (IS) where it is properly analyzed. The power factor of the converter is 0.9997 that is very high. It showed that

it could utilize the input electric energy without distortions very well. Additionally, the Total Harmonic Distortion (THD) is still remarkably low at 1.18%, demonstrating the converter's ability to maintain excellent power quality.

To further explore the system's response, the Fast Fourier Transform (FFT) of the system was calculated, as shown in fig. 5(b), which reveals the powerful effect of the proposed Proportional-Integral (PI) control strategies. The level of THD is always at a very low level, which again demonstrates the superiority of this system over other systems, and its ability to significantly reduce the level of harmonic distortions. In conclusion, these findings highlight the converter's capability of providing stable and distortion-free power delivery, contributing to the reliability and efficiency of the system.

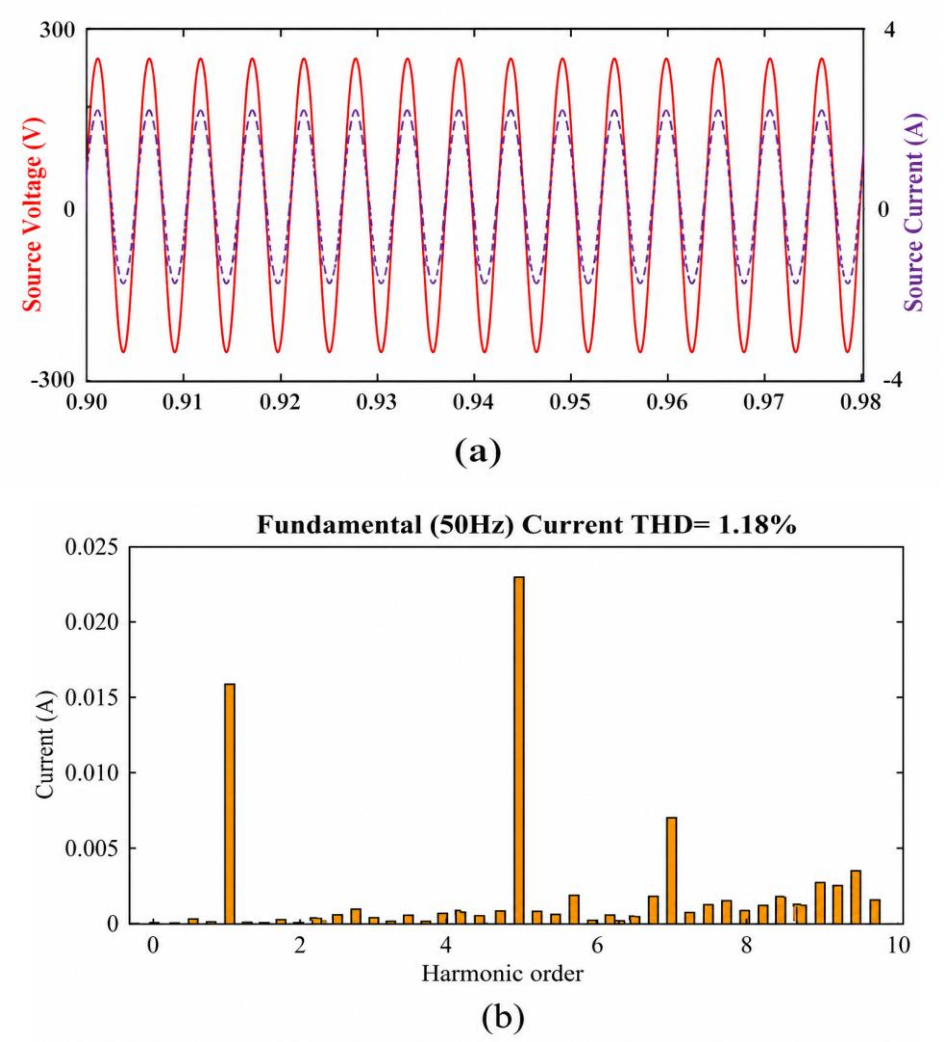


Fig. 5: Simulated Analysis Showcasing the Operational Efficiency of the Optimized Converters Under PIM Control at an Input Voltage of 230v. (a) Visualization of Steady-State Waveform Characteristics Observed at the Source Terminals. (b) Frequency Domain Analysis Emphasizing the Harmonic Spectrum and Computed Total Harmonic Distortion (THD)

The dynamic response of the proposed converter under varying energy demand conditions is shown in fig. 6(a) and (b). Since the system is very versatile, it is stable to abrupt load variations which makes it suitable to the practical usage where load is variable unpredictably. Performance index for PIM, such as settling time, rise time and peak overshoot, is examined and evaluated with quite nice results. From the plot we could get the rise time less than 0.01 s, the peak overshoot as 1.32% and settling time as 0.095 minute. Those are the remarkable advantages over other control system. All the results are summarized to table 5 to make the comparisons simple and fast.

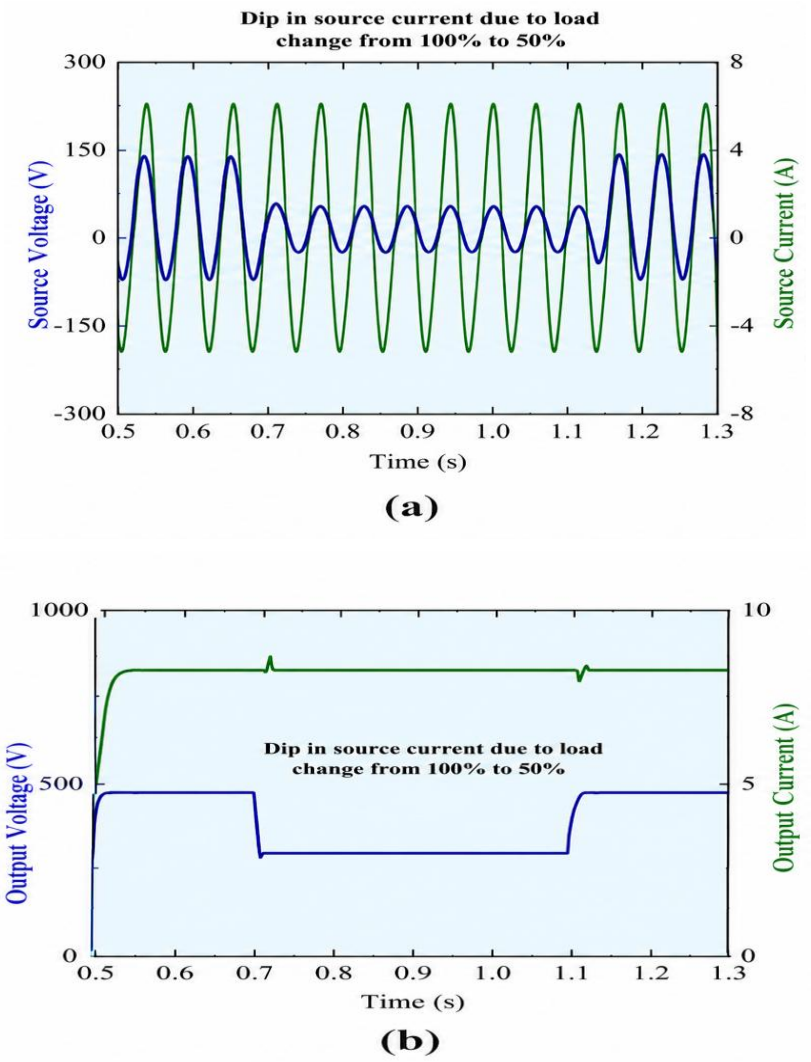


Fig. 6: Simulink Analysis of Enhanced Conversion Efficiency Utilizing PIM Control at V_S = 230V (a) Load Voltage (V_L) and Load Current (I_L) at 50% Load Operation, (b) Source Voltage (V_S) and Source Current (I_S) at 50% Load Operation

Detailed investigations have been carried out over how different load conditions affect various PQ parameters, output stability and the current consumed by the circuit under a rated supply voltage of 230V. These investigations are presented in graphical form, by relating the same on varying load condition, in fig. 6(b), and it reveals much more in interpreting the behavior of the controller over different load conditions. The simulation results very strongly support the conclusion that optimal PIM under different energy supply condition are remarkably consistent and stable. The proposed controller is found to be adaptable very fast and a well-performing candidate for all highly efficient PFC application.

The experiments on varying load ratio in Wide-Loop configuration are tabulated and their respective results are summarized in table 2. table 2 displays critical findings of how the load cycles vary depending on the condition of the system and gives us an idea how the system is performing under varying loads. The system is further analyzed for its voltage source deviation; this allows for greater insight into the efficiency and the robustness of the system as we move towards the Close-Loop evaluation phase.

Table 3 details precisely the observed validated set position energy fluctuations gained from closed-loop tests. These fluctuations provide the robust validation to confirm the effectiveness of the controller at holding its set point energy value constantly at desired values. Table 3 provides an excellent visual representation of how the controller responded to the set position energy step changes in all different operating modes.

These tables are organized lists of system parameters and control implementation. The obtained results are of significant importance for the system's dynamic behavior which will further enable the development of control algorithms for similar applications. Table 4 is a breakdown of the converter system power dissipation, illustrating an in-depth analysis on power loss of each component of the converter system. Measuring power loss is a crucial factor for the overall efficiency and thermal behavior of a power electronics device, with the overall system loss equal to the sum of all losses. Classifying and identifying all the loss components helps to determine points of improvements.

Aside from being a high-performance controller for its steady state performance, the presented method of control is deeply investigated to demonstrate its resilience to AC input voltage variations in terms of its dynamic response. The presented controller is demonstrated in table 5 to operate with more efficiency compared to some traditional systems; and is demonstrated to effectively mitigate electrical disturbances. Empirical data indicates not only the power of oscillation attenuation of the controller, but it has been identified the controller has an opportunity to do better compared to present power control methodologies for power control.

The prototype is laid out onto a 4-layer FR4 board (size 150mm 100mm). The power stage (MOSFETs SA, SB and diodes DE, DF) is placed in the top layer and has a solid copper pour connected to improve cooling. The gate driver and the DSP board (TMS320F28379D) is mounted onto a separate control board with an isolated interface. The inductance LA (2 mH, Litz wire, PQ50/50 core) and capacitance CA (400 F, 900 V) are mounted on board as there was not enough space on the prototype board. Snubbers are fitted to each switch on the board to damp voltage spikes.

Table 2: Variations in Duty Cycle Under Open-Loop Operation

Duty Ratio	V_S (V)	I_S (A)	V_L (V)	I_L (A)	THD (%)	PF	Efficiency (η) (%)
0.25	230	3.47	80	8.87	15.9	0.89	88.7
0.5	233	3.43	699	0.99	23	0.83	87
0.75	237.5	3.37	712.5	0.97	23.5	0.83	86.3
0.8	242	3.30	726	0.98	16.6	0.892	89.2

Table 3: Evaluation of Closed-Loop System Dynamics Under Fluctuating Reference Voltage Conditions

Reference Voltage (V)	Source Voltage (V)	Source Current (A)	Load Voltage (V)	Load Current (A)	Power Factor	Source Harmonics (%)	Efficiency (%)
630	230	3.47	625	1.18	0.9993	1.28	92.9
660	230	3.47	662	1.16	0.9995	1.23	96.2
690	230	3.47	690	1.13	0.9997	1.18	97.5
720	230	3.47	720	1.07	0.9996	1.25	96.30
750	230	3.47	752	1.02	0.9996	1.25	96.6

Table 4: Breakdown of Power Losses for 97.5% Efficient System (800W Power Rating)

Loss Category	Type of Component	Percentage Contribution (%)	Power Loss (W)	Description
DBR Losses	Diode Bridge Rectifier	31.2%	6.24 W	Losses due to rectification process, mainly from conduction and switching effects.
MOSFET Losses	Power Switch	24.7%	4.94 W	Conduction and switching losses in the MOSFET, affecting conversion efficiency.
Diode Losses	Semiconductor Diodes	12.3%	2.46 W	Power dissipation from forward voltage drops and reverse recovery effects.
Inductor Losses	Magnetic Component	6.9%	1.38 W	Core and copper losses in the inductor due to energy transfer.
Capacitor Losses	Energy Storage Element	6.5%	1.30 W	Dielectric and ESR-related losses in capacitors, influencing stability.
Filter Losses	Passive Components	5.9%	1.18 W	Losses due to resistance and reactive power effects in filter circuits.
Miscellaneous Losses	Other Components	12.4%	2.48 W	Losses from auxiliary circuits, connections, and minor inefficiencies.
Total			20W	

Table 5 depicts the thorough evaluation and comparison of MGBBPFI converter against the conventional PFC topologies, covering various critical performance parameters such as the input voltage range, power rating, conducting scheme, voltage gain, efficiency of conversion and the Total Harmonic Distortion. The comparison shows that this converter exhibits excellent performances characterized by efficient energy utilization, diminished switching stress and improved power quality.

Table 5: Performance Comparison of Proposed MGBBPFI and Conventional PFC Converters

Parameter	(Kumar & Verma, 2021)	(Maghsoudi & Farzanehfard, 2023)	(Singh et al., 2024)	(Vijayakumar & Sudhakar, 2024)	(Annambhotla & Parthiban, 2022)	MGBBPFI (Proposed)
Input Voltage Range (V)	110-230	90-130	160-260	220	230	85-265
Output Voltage (V)	55	48	36-72	60	54	48-400
Power Capacity (kW)	1	0.12	0.45	0.46	0.15	1.0
Conversion Elements	6S, 6D, 3L, 3C	3S, 4D, 1L, 1C	3S, 5D, 2L, 4C	1S, 5D, 2L, 2C	1S, 7D, 4L, 4C	2S, 6D, 2L, 2C
Control Scheme	Discontinuous Mode (DCM)	DCM	DCM	CCM	CCM	Continuous Mode (CCM)
Efficiency (%)	92.8	96.2	92.1	97.8	80	97.5
Switch Stress (V)	M	M	L	L	H	L
Power Factor @ FL	0.99	0.98	0.99	0.9998	0.92	0.9997
THD @ FL (%)	2.6	4	3.5	1.75	2.8	1.18
Total Component Count	18	9	14	10	16	12
Estimated Relative Cost (p.u.)	1.5	1.0	1.3	1.1	1.4	1.05
S – Switches | D – Diodes | L – Inductor | C – Capacitor | FL – Full Load | H – High | L – Low | M – Medium						

Switch Stress classification. The level of the switch stress is defined by the normalized voltage stress across the power switch as Vstress / Vout. This MGBBPFI converter shows that $V_{\text{stress}}/V_{\text{out}}$ ≈1.3 (calculated as $V_{\text{out}}/(1-2D)$, where D<0.5), which fall in to the Low (L):(<1.5) stress class.

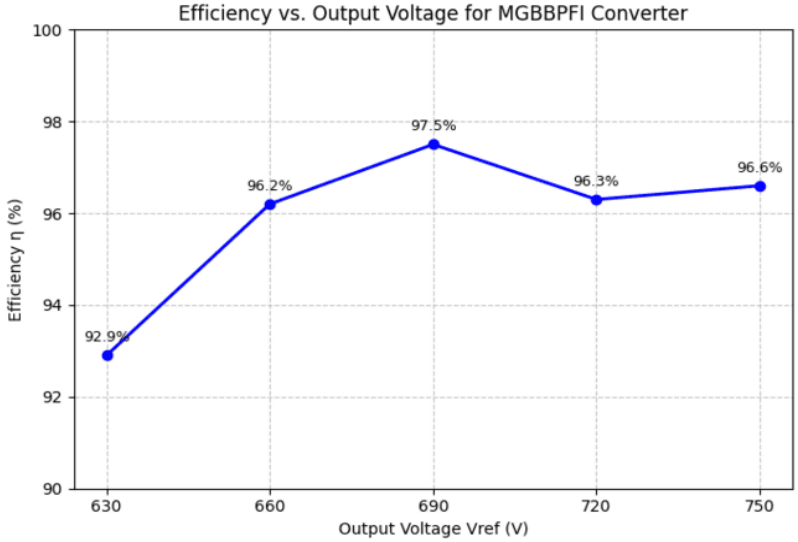


Fig. 7: Efficiency vs. output voltage

The behavior of converter efficiency is dependent upon the output voltage Vref, presented in fig. 7. A maximum of 97.5 % at Vref = 690V with a relatively slight degradation for higher output voltage and minimum of 92.9% at Vref=630V. This graph provides us the best point and behavior of the converter with regard to voltage and offers the possibility to observe converter dependent performance of load.

Table 6: Converter Performance Metrics Under Varying Load Conditions

Load (%)	Output Power (W)	PF	THD (%)	Efficiency (%)
25%	200	0.998	2.1	94.2
50%	400	0.9995	1.45	96.4
75%	600	0.9997	1.28	97.1
100%	800	0.9997	1.18	97.5

Table 6 represents a summary of the key performance indicators for the MGBBPFI converter, for several load percentages: It consists of output power, power factor (PF), total harmonic distortion (THD), and conversion efficiency. The data illustrate that the converter operates at high PF, low THD and peak efficiency at full load but has a marginal variation at partial loads, indicating high stability and efficiency of the converter throughout the tested load range.

Performance Metrics

1. Power Factor (PF)

The input current efficiency ratio is given by Equation (19) which is a measure of the efficiency with which the input current is used to generate useful power. It is the ratio of real power (P) to apparent power (S). It can also be written as the cosine of the angle of the phase angle multiplied by the ratio of the fundamental input current I_1 to the total RMS current I_{rms} using harmonics.

$$\text{PF} = \frac{P}{S} = \frac{V_G \cdot I_G \cdot \cos\ \phi}{V_G \cdot I_G} = \cos\phi \cdot \frac{I_1}{I_{\text{rms}}} \tag{19}$$

2. Total Harmonic Distortion (THD)

The expression in equation (20) is a measure of the distortion of the input current caused by harmonics other than the fundamental. It is defined as the percentage of the RMS value of all the harmonic currents (I_n, $n \geq 2$) against the fundamental current (I_1):

$$\text{THD}(\%) = \frac{\sqrt{\sum_{n=2}^{\infty} I_n^2}}{I_1} \times 100 \tag{20}$$

3. Conversion Efficiency (η)

Efficiency is the ratio of output power to the input power. For a converter, it is defined by the ratio of output power ($P_{\text{Output}} = V_L \cdot I_L$) to the input power ($P_{\text{Input}} = V_S \cdot I_S$) in percentage as outlined in equation (21):

$$\eta(\%) = \frac{P_{\text{Output}}}{P_{\text{Input}}} \times 100 = \frac{V_L \cdot I_L}{V_S \cdot I_S} \times 100 \tag{21}$$

4. Voltage Ripple ($\Delta V_L/V_L$)

The voltage ripple is the voltage variation from the nominal output voltage. Using the peak-to-peak ripple $\Delta V_{L_{pp}}$, it is expressed as a percentage as shown in equation (22):

$$\frac{\Delta V_L}{V_L}(\%) = \frac{\Delta V_{L_{pp}}}{V_{L_{\text{nominal}}}} \times 100 \tag{22}$$

Taken together these indicators show the converter as a whole, its efficiency, quality of waveforms, stability.

Conclusion

This work presents an advanced MGBBPFI (Improved Gain Buck-Boost Power Factor Correction) converter, which effectively overcomes the limitations associated with conventional AC-DC conversion stages. The presented topology provides not only enhanced regulation, stability and power quality, but also exhibits a fast dynamic response and low power overshoot. In order to validate the proposed design, extensive MATLAB/Simulink simulations and a hardware implementation of a prototype of 800 W were undertaken. The converter was found to perform remarkably well under various operating conditions and is robust against sudden load and voltage variations. A near-unity power factor, a low THD of 1.18%, and a high efficiency of 97.5% were recorded, making the converter superior to all the contemporary designs. The obtained results show tremendous promise in this field, as they offer a reliable and stable solution for different power conversion applications, such as renewable energy systems, EV charging systems and industrial power supplies. Future research on this project is suggested: (i) extending the MGBBPFI topology in a three-phase interleaved configuration for higher power applications (>3 kW) targeted toward EV charging, (ii) investigation into model predictive control (MPC) as an alternative to PI-PR dual-loop control and its benefit on reducing THD under abnormal grid conditions, (iii) realization of wireless power transfer (WPT) capability by integrating a resonant coil network with the converter output, (iv) thermal management optimization for automotive applications operating at high ambient temperatures (>85C), and (v) implementation on a GaN-based switch to further reduce the passive component sizes by increasing the switching frequency over 200 kHz.

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