International Academic Institute for Science and Technology

International Academic Journal of Science and Engineering
Vol. 1, No.2, 2014, pp. 96-105.
ISSN 2454-3896

International Academic Journal of Science and Engineering

www.iaiest.com

A low power and high gain CMOS LNA for UWB applications using a gate inductor

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Abstract

A new ultra wideband low noise amplifier is presented.The ultra wideband LNA consists of two simple amplifiers. A common source topology by gate inductor is adopted for input stage to achieve wideband input matching and wider bandwidth. The second stage by noise cancelling technique achivies high flat gain .Realized in standard TSMC0.18μM CMOS. It achieves a maximum power gain of 11.8 dB, a bandwidth of 10GHz and 4.9dB minimum noise fiqure.The power consumption is 22mW from a 1.8v supply.

Keywords: UWB,CMOS,gain-flatness,Noise figure,low noise amplifier.

Introduction:

In recent years, the Federal Communications Commission (FCC) in the US approved the use of ultra-wideband technology for commercial applications in the 3.1-10.6 GHz. UWB performs for high-speed uses such as wireless personal area networks, medical-imaging systems,ground and vehicular penetrating radars and high-speed indoor networking[1-6].

LNA as the first module of UWB receiver has important influence on the sensitivity and dynamic range of the whole receiver system.LNA needs to features such as broadband input matching to minimize the return loss,sufficient gain to suppress the noise of a mixer,low noise figure to enhance the sensitivity of a receiver,small die area to reduce the cost and low power consumption[2-7].In addition the LNA input impedance should be close to 50Ω across the band from 3 to 10 GHz.

Many topologies have been presented in LNA designs,such as cascade amplifiers,distributed amplifiers, current-reused amplifiers and feedback amplifiers.The distributed amplifier provide good linearity and sufficient matching conditions and improve gains at higher frequencies.The resistive feedback has

advantage such as gain flatness, noise figure and matching and it tends to degrade the noise performance because of the feedback resistor peak near the input stage.

This paper introduces a gate inductor to achieve high and flat gain and wider bandwidth.The gain S21 is approximately equal to 11dB and the minimum NF is below 5 dB in the entire band.

The paper is organized as follows. Section 2 shows proposed UWB LNA.Section 3 analyes the proposed LNA and section4 gives the simulation results and compares its performance with recently reported CMOS LNAs.

CIRCUIT DESIGN OF UWB LNA:

The schematic of the UWB LNA is shown in Fig.1. In the proposed UWB LNA,a resistive feedback and gate inductor are adopted in the first stage for bandwidth enhancment and input impedance matching, while a noise cancelling technique is adopted in the second stage for high gain.

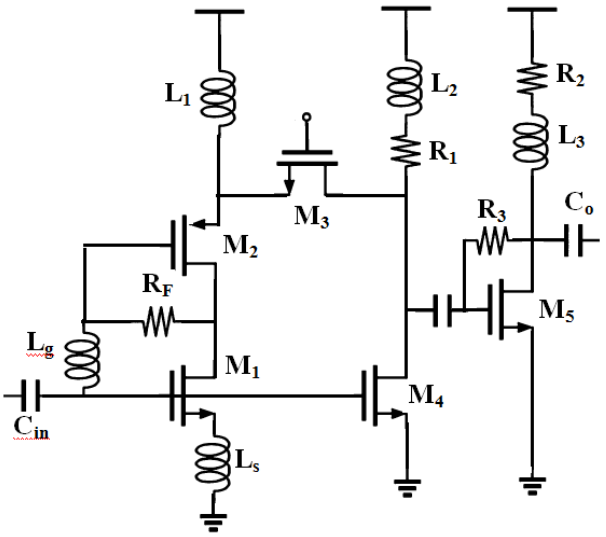


Fig.1.The proposed UWB LNA

ANALYSIS OF PROPOSED UWB LNA:

The small signal equivalent circuit of the first stage is illustrated in Fig.2. The circuit of proposed UWB LNA is shown in Fig.1, which is composed of two simple amplifier.The main problem with the use of resistive in LNA is that the parasitic capacitances due to the miller effect, and hence lead to degradation in input impedence at high frequency.

For input matching, the LC network combined with the Lg and the intrinsic capacitances to form a LC ladder network for achieving a wideband matching.
Assuming that the input miller effect is relatively small.

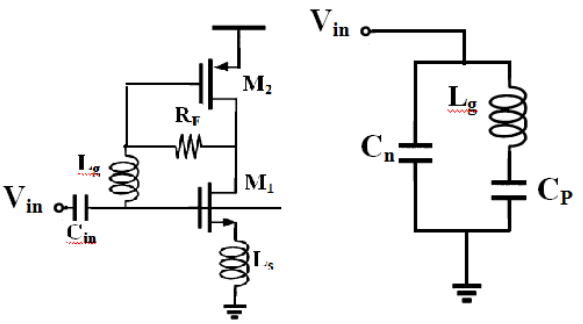


Fig.2 gate inductive topology and equivalent model

As can be seen in the equivalent ac model,the L_g inductor split the parasitic capacitance(C_{gs} and C_{gd}) at the input of amplifier and facilitates bandwidth extension.
Input impedance of the proposed LNA can be expressed as

(1)

(2)

Assuming R_F is small.therefore Z_{in} is given by

$$\frac{\|(r_{o1}\|r_{o2})}{\left(\frac{}{1(r_{o1}\ \ o2)}+\frac{}{2(r_{o1}\ \ o2)}\right)} \quad (3)$$

Fig.3 illustrates the effect Lg on the input impedance.

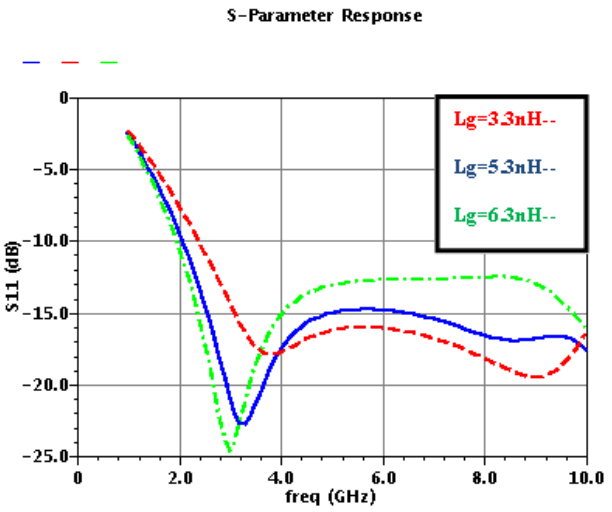


Fig.3 effect Lg on the S11

Fig.4 illustrates the effect L_g on the gain. The gate inductor is connected in series to parasitic capacitance and forms LC network.where $\omega_0 = \frac{}{\sqrt{L}}$ and $Q_0 = \omega_0 L_g / R_{L_g}$.

When ω is lower than ω_0, the signal at M_1's gate is amplified.
Therefore,a wider bandwidth and flat gain is available.
When ω_0 is near to lower than ω_p an overpeaking of gain will occur and it may lead to stability issue.on the other side when
ω_0 is higher than ω_p, the LNA cannot get effective gain.
M_3 and M_4 are used to combine the signal and subtract the noise of M_1.By adding M_3 the part of current of M_3 flows into M1, which increases gm1. The amplifier AX is implemented in a common-source configuration by M4 and AY is implemented
in a common-gate configuration by M3. AX and AY are expressed as[11] .

(4)

(5)

(6)

(g) (7)

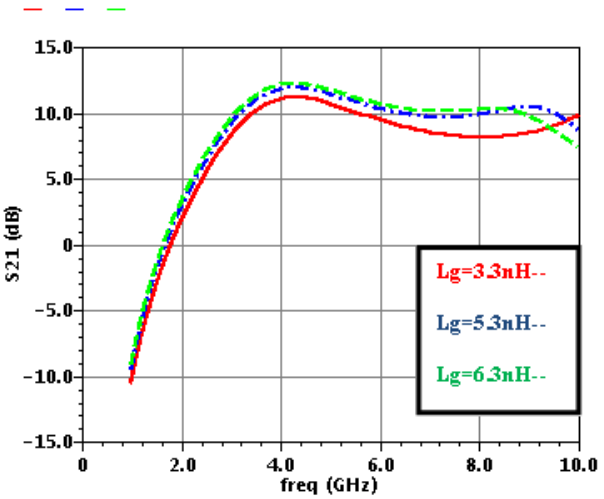


Fig.4. effect Lg on the S21

The main noise source in this LNA are the channel noises of M1 and M2 and the thermal noise of the feedback resistor RF.

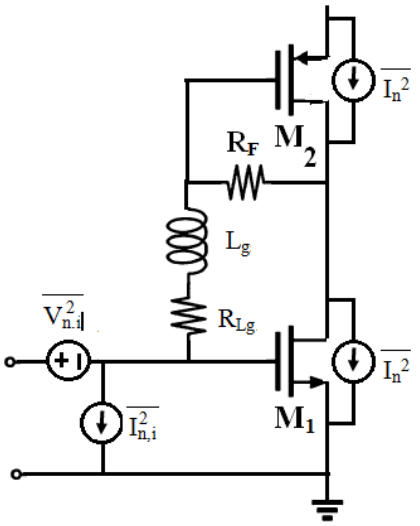


Fig.5. model transistors thermal noise

Modeling the channel thermal noise of M_1 by a current source between drain and source $I_{n,M1}$ is defiend as

$\overline{I^2}$ = – (8)

ϒ is a noise parameters and $\alpha = g_m/g$, where is the channel conductance for V_{DS}=0.
The noise factor F can be derived by [5]

(9)

$\overline{V^2}$ (10)

$\overline{I^2}$ = (11)

Fig.6 illustrates the effect L_g on the noise fiqure.

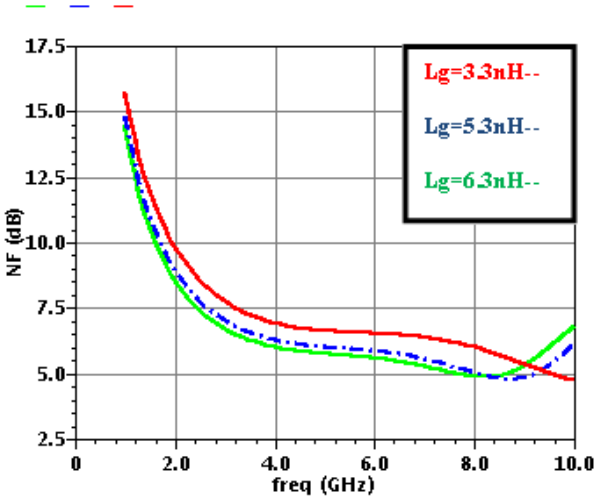


Fig.6. effect Lg on the NF

SIMULATION RESULT :

Fig.7 shows the simulated results of input reflection coeffient(S11) .The simulared S11 is lower than -10 dB over the entire3.1-10.6 GHz. The simulated results of output reflection coefficients (S22) is shown in Fig.8. The S22 is less than -10 dB. Fig.9 shows the simulated gain.The maximum S21 is 11.8dB.Fig.10 indicates the simulated reverse isolation (S12) for the UWB LNA circuit.An S12 is less than -35dB.The simulated NF is shown in Fig.11 and minimum NF is 4.9dB. The proposed circuit cosumes 22mW from 1.8V supply voltage. The component values of our proposed circuit are also shown in Table.1.Table 2

summarizes the performance of the LNA and compares with the other reported circuit performance.The proposed circuit shows a good performance with low power , high gain and low noise.

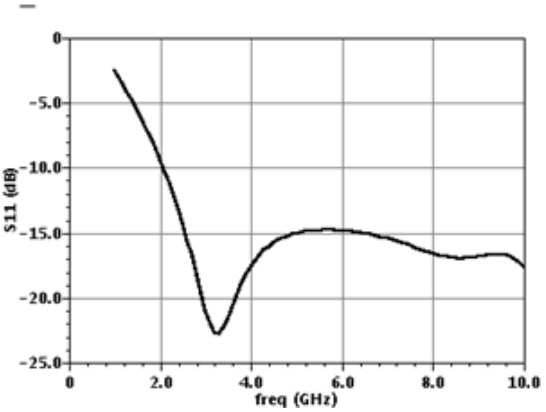


Fig.7.simulated S11

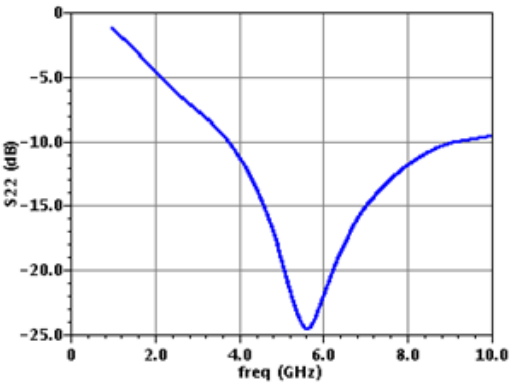


Fig.8.simulated S22

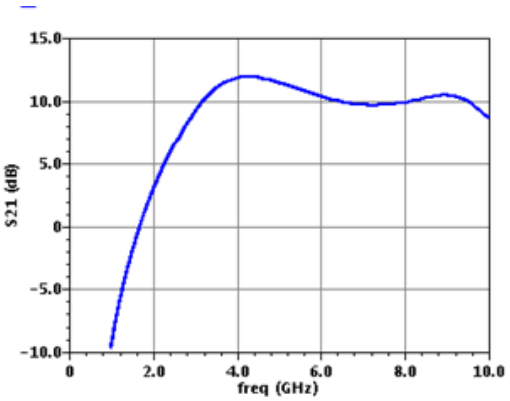


Fig.9.simulated S21

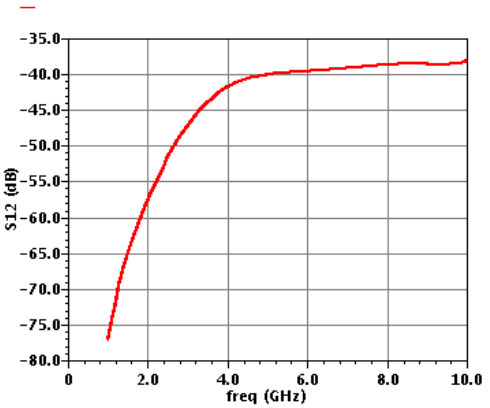


Fig.10.simulated S12

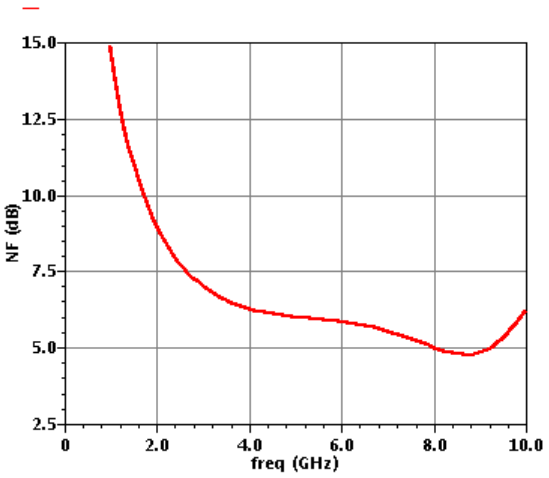


Fig.11.simulated NF

TABLE1-Component values of the LNA

Transistor size	**$(W/L)_1$**	**$(W/L)_2$**	**$(W/L)_3$**	**$(W/L)_4$**	**$(W/L)_5$**
	260/0.18	110/0.18	36/0.18	80/0.18	60/0.18
Inductor value	**L_g**	**L_s**	**L_1**	**L_2**	**L_3**
	5.3nH	0.7nH	6.1nH	6.5nH	1.9nH
Resistor value	**R_F**	**R_1**	**R_2**	**R_3**	-
	200Ω	75Ω	56Ω	1.5KΩ	-

TABLE2-Preformance of the proposed UWB LNA and comparison with other UWB LNAs

Reference	[9]	[10]	[11]	[12]	This work
Technology	90nm	0.13µm	65nm	90nm	0.18µm
BW(GHZ)	1.6-28	1-10.6	1-10.5	0.5-8	3.1-10.6
P_{dc}(mw)	21.6	26	36	42	22
NF_{min}(dB)	2.92	2.3	3.9	1.9	4.9
S_{11}(dB)	<-10	<-12	<-10	<-7	<-14.8
G_{max}(dB)	10.7	16	16.5	22	11.8
FOM	20.8	8.46	2.99	7.1	1.9

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