International Academic Institute for Science and Technology

International Academic Journal of Science and Engineering
Vol. 1, No.2, 2014, pp. 133-151.
ISSN 2454-3896

International Academic Journal of Science and Engineering

www.iaiest.com

Multiprocessor capabilities and increase the processors' numbers used in PCs (Dual Board in PC)

SeyedJavad Azimfar[a]

[a]*Master of Information Technology Engineering, Tarbiat Modares University, Tehran, Iran.*

Abstract

First, in order to access parallel processing by PCs, it is necessary to provide an environment for data communication between them. The computer networks are the most common communication way between computers. So, many researchers tried to create a parallel processing system via current common computer networks. With preparing hardware system, there is just need for a favor software environment to operate processing. The networks are not designed for it, so caused many limitations naturally. In this article tried to review a plan in order to overcome the limitations and to create multiprocessor in standard feature of personal computers (ATX), it causes to achieve high speed in PCs. The plan is derived of Pentium 2/3 Xeon processors model which have been analyzed. Also, the article is considered the simulation model based on Proteus software. CPU and RAM in this simulation used for the function and architecture between them ,also the manner of multiprocessor is considered in PC-motherboard; and its hardware model is designed in the article.

Keywords: Multiprocessor, Parallel processing, Simulation and Proteus.

Introduction

In all over the world as long the people were desired to use the parallel computers because they are believed the next generation of computers will be acted as parallel. According to advanced science and engineering, more details through new applied models will be provided to enhance the need for storage computing and capacity. Various methods have been used to increase computer speed included a processor parallelism. It is such as superscalar by pipeline method or multiple execution units, coherent operation of various units and accelerated arithmetic & logic unit or used time or data parallelism. Also, multiprocessor is designed through using parallelism for problem solving and computing to increase computer speed. Multiprocessor computers were created as super-computers then current servers. As we know, computing and difficult problems are solved by engineers and designers by using PCs. With increasing of personal computers speed ,it will easy and fast to solve problems. It is so important to know how could increase personal computers speed based on more servers progression. But, first should be known about all PCs' limitations and standards to increase their speed then used in designs. The designed model is introduced and practiced in this article.

Proposed Model

In proposed model tried to follow all components from PCs-motherboards standards, and our purpose is very high speed of processing in PCs' motherboards; the processors board is separated of motherboard. Motherboard will be

connected to main board via connective board as called Daughter board. The aim is to use servers' technology in PCs' motherboards sorts. In this article
some cases will investigate include; used and CPU arrangement and their connection to motherboard, architecture and provide the Block Diagram, calculating power, temperature and issues related to that, and amount of speed ratio and/or acceleration or Random.

Investigation of motherboard and CPU used at the model:

In the article we will use from Pentium 2/3xeon processor, because the CPU architecture is close to desired model. In the article there is no infrastructure technology, so we have to use some models for technology and processors and etc, to provide it. First, we will consider the replacement method of a processor on motherboard , figure 1 is shown a processor type and its receiving motherboards used in model. According to figure 1,[47], CPU located into own slot vertically.

The choosing reasons this model are:
1. Vertical CPU location
2. Ability of components' arrangement, order and sequence on motherboard
3. Use of several CPU on CPUs board and increase the speed

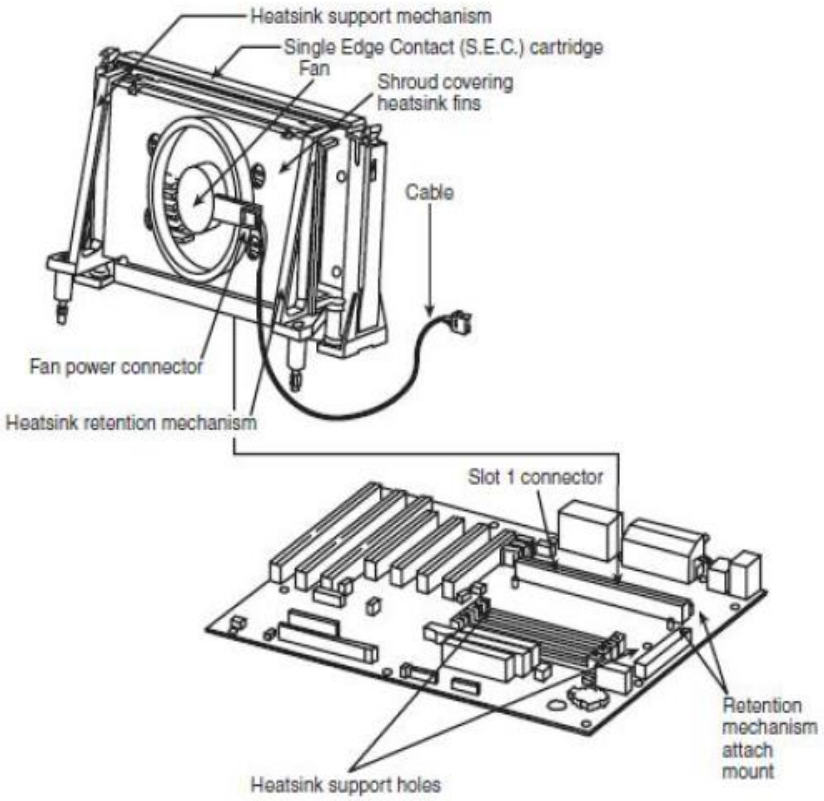


Figure 1. Pentium 2/3 Xeon location

We refer to the proposed model and follow the discussion. In the model, Daughter board installed a board on motherboard to establish CPU. However, it is created more spaces to install CPUs, but caused to enhance more maneuver on motherboard through empty them. Dual Board is a favor name for that. Because it is divided to two separated boards included CPUs and motherboard. If we want to have consider the motherboard dimensions as the same ATX there is need to install about 4-5 CPU on CPU board and connect to motherboard by Daughter board. It is necessary to remain some notes about the proposed model. As we know, the motherboard is exactly the same motherboard that Pentium 3 Xeon can be installed on it. About 4-5 or more slots are located to install CPU on it and there are at the same or more Ram slots to provide the distributed memory architecture completely.

CPUs' arrangement and their relationship to motherboard in the model

At this section, the servers included two CPU to use Pentium 3 Xeon as motherboard processors are from 1999. Before 2000, the sizes of some server's motherboards were the same ATX for home and administration applications as see following. According to the model at this section can discuss about CPUs' arrangement and their relationship to motherboard. It is tried to estimate the CPUs' volume and existing space ,then arrange them based on these cases and the distance of CPUs and RAMs at this model.

CPUs board ' s model

CPUs are located on a board which is exactly as like as motherboard will be connected to motherboard by Daughter board. So, it is caused the applied processors and finally its speed become more. The board and installed processors on it are showed in figure 2.

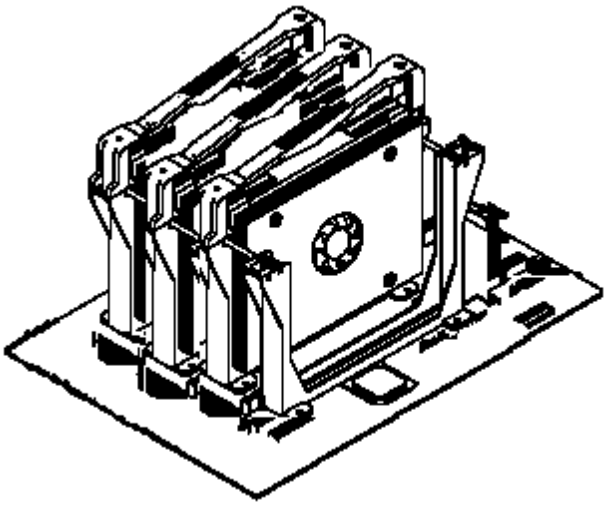


Figure 2. CPUs board

Daughter board in the model

It is as Daughter board included two sides which installed into motherboard in one side and CPUs board on the other side. It is ability to transfer data from CPUs to RAM (and versus) and also can help to supply power for CPU. The board is shown to connect the motherboard and processors board in figure 3.

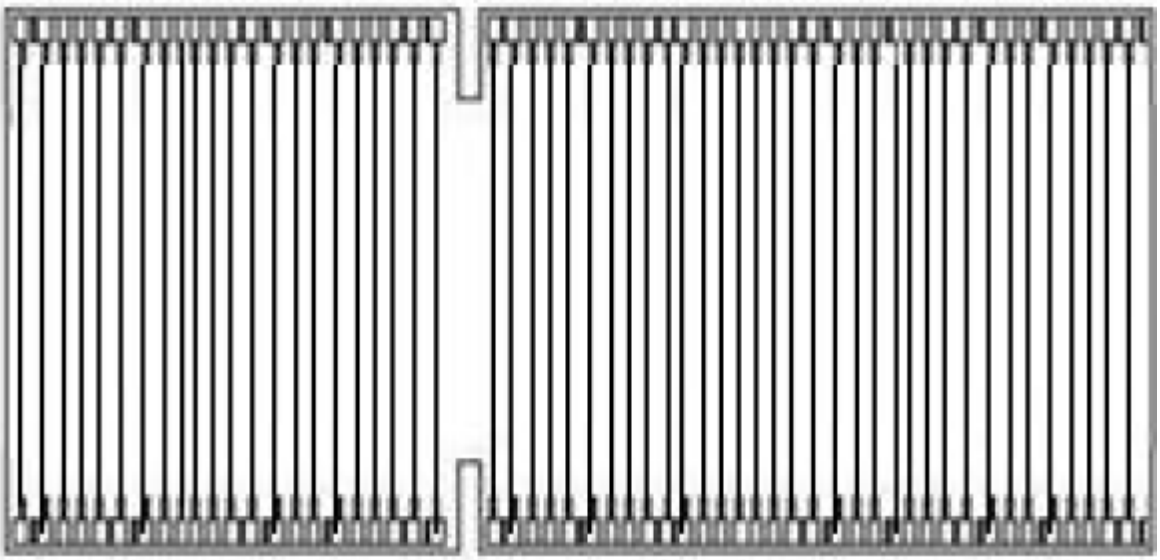


Figure 3. Daughter board

If we have supply power for CPUs separately, so there is no need for Daughter board to supply power and it will be used just for data transferring. Figure 4 is shown the Daughter boards arrangement.

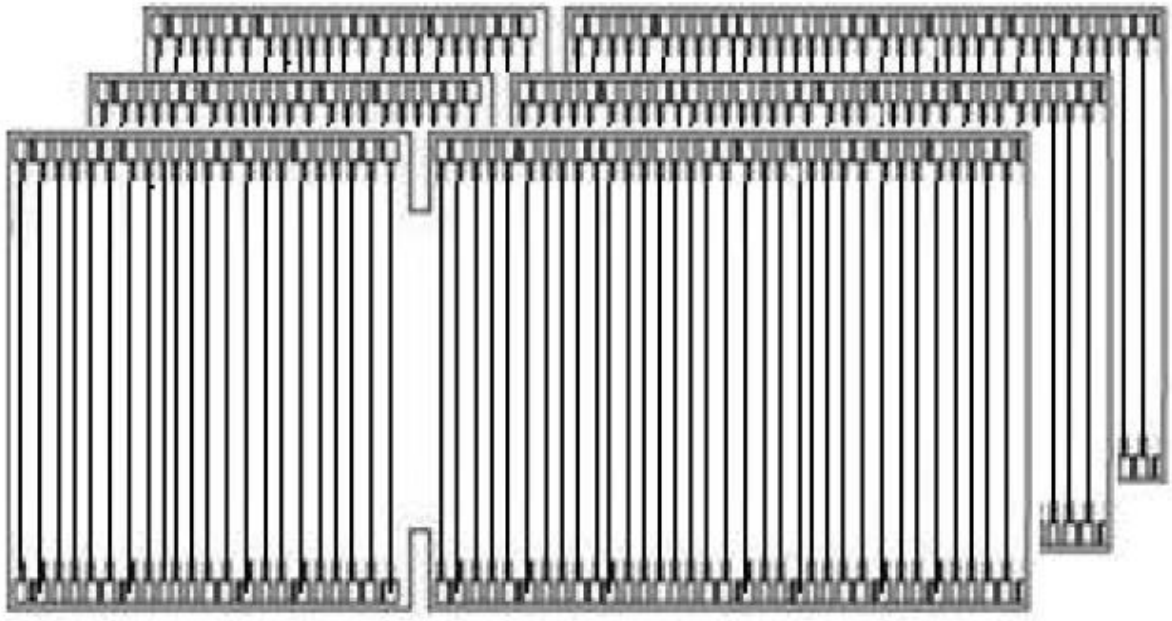


Figure 4. The Daughter boards arrangement

Implementation

The hardware made by me and is acted after final model implementation (figure 5). As noted, CPUs boards are connected to main motherboard by Daughter board.

It causes several CPU used by CPUs board with more ability to increase processor speed.

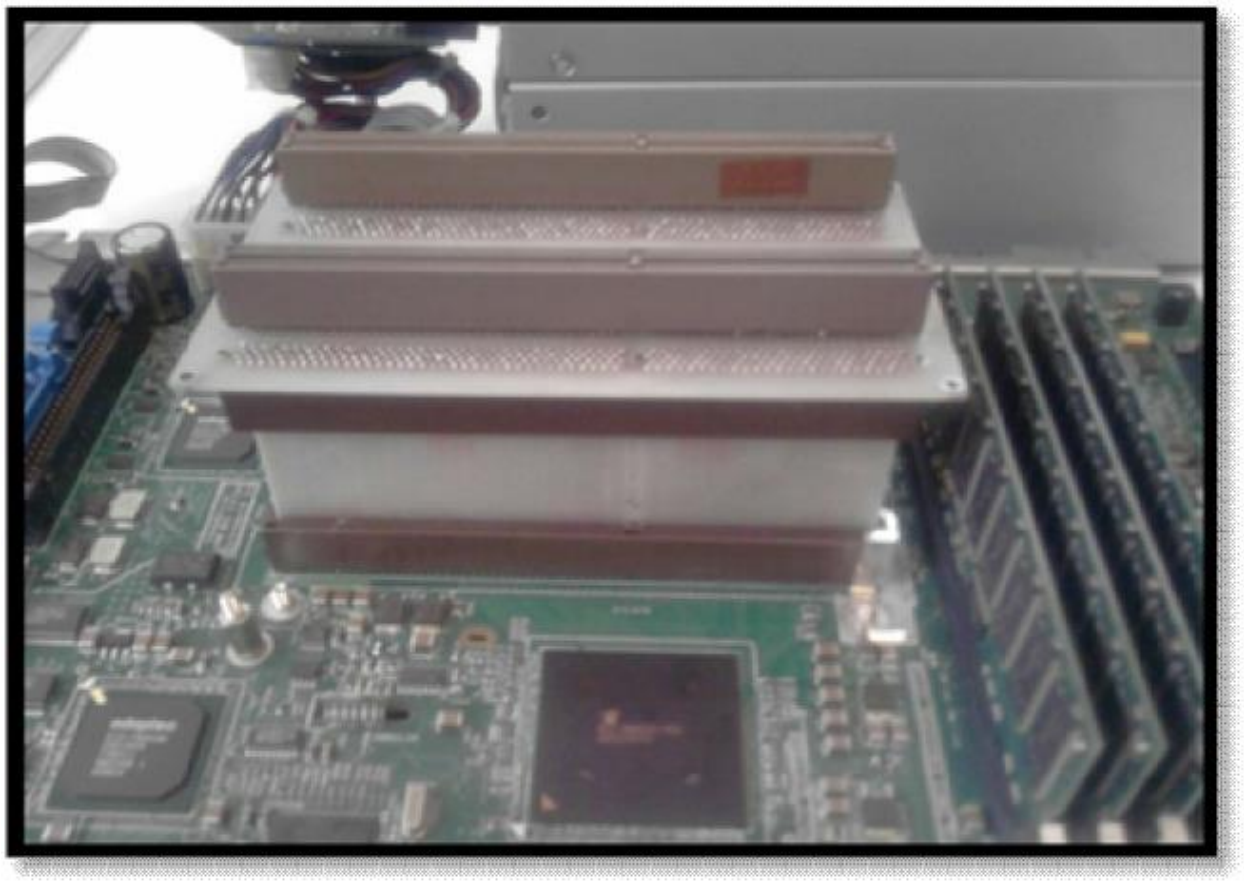


Figure 5. The hardware

Segments dimension

There is mentioned various standard segments dimension of PCs' motherboards by appendix. According to that, graphic cart slot distance (last slot into motherboard) and motherboard edge is about 6.25", it is RAMs and CPUs' field. The field based on the dimensions and CPU and also Daughter board as connective board may know as a CPU and RAM triggering and installing field.

Some notes about dimensions

As mentioned, there is a space about 6.25" in length and 8.95" in width to install the RAMs and Daughter boards and also north bridge and some connectors. To install the CPU board in this space there are two reasons :

1. the distance of CPUs to north bridge (not more 15")
2. have no disturb of graphic carts and all PCI/PCI-E length

As it estimated, approximately the RAM maximum height is about 3cm and also the maximum of north bridge height is about 2.9 cm based on new coolers (copper tube), so Daughter board height must be more than 3 cm. *H(Ram)=3cm , H(n .b &cooler)=2.9cm < H(Daughter board)*

As we know, the graphic cart height and other slots carts are more than 11 cm , therefore the location of installing CPU board must not be involved into slots field.

Architecture and its processing

According to the model tried to use among of multiprocessor architecture that:

1. To have more performance than other.
2. To have less complexity

3. To have more operating efficiency and acceleration

According to architecture, the distributed memory architecture is purpose. In relating to that, each CPU have its own RAM; processing acted separately and then results will be returned. Figure 6 is shown the buses applied in motherboard will be connected to RAMs through processors' north bridge. As mentioned before, the program is divided to concurrent processes as applicable program which acted into separated processor. If there are more processes than processors, it needs a processor act more process in time shared model.

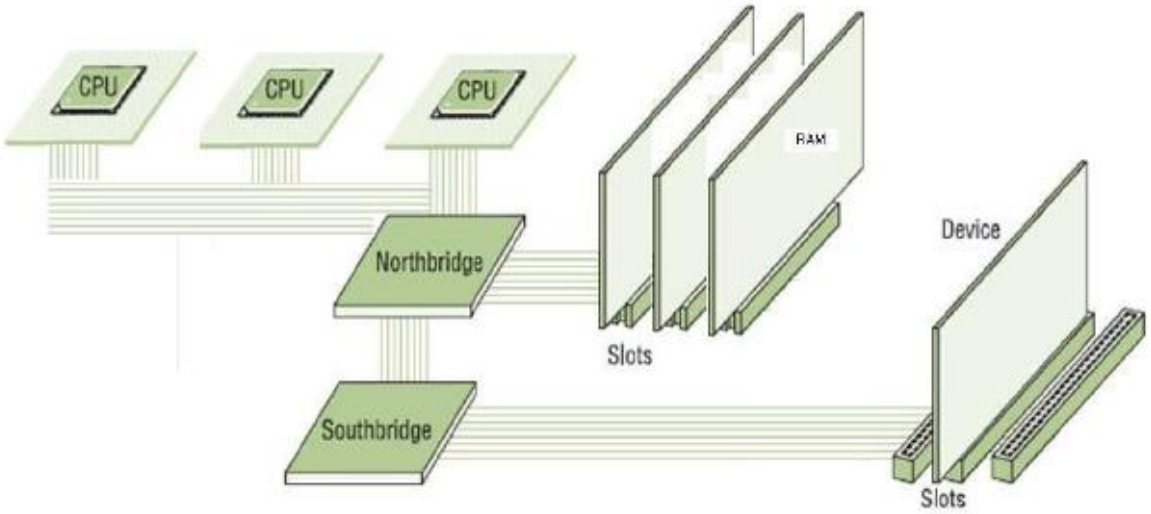


Figure 6. Motherboard buses

The implemented processes on a processor transferred a message across themselves by using of inner channels. There is shown a perfect operation processing act into a processor and its relationship to main memory in figure 7.[49][50]

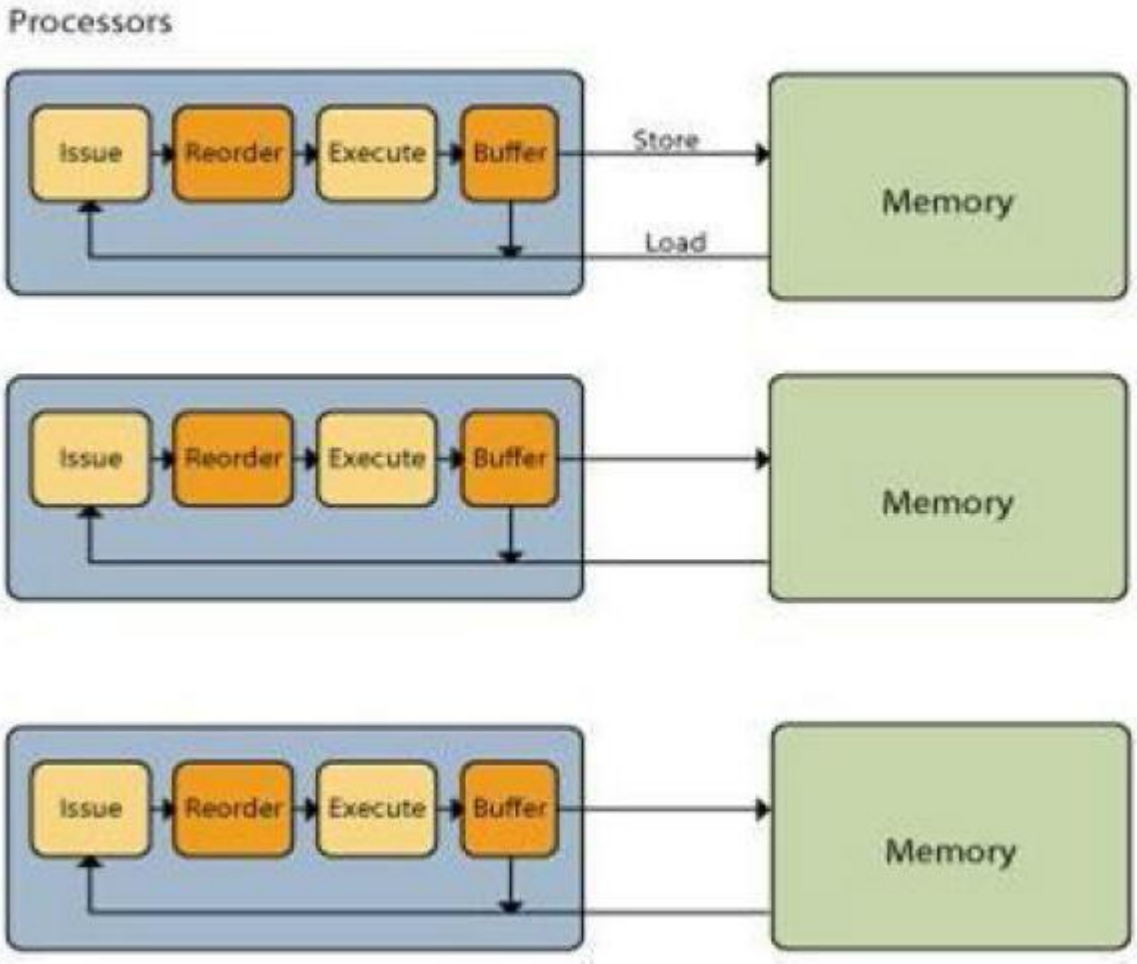


Figure 7. CPU and RAM relationship

The processes are used inner channels for massage transferring after they implemented on various processors. It is not possible to share transferred data across the processors. They copied (by sender/receiver message). No need for synchronization structures such as semaphores is the most important benefit to improve operation instead of data transferring. In addition, it is so flexible to arrange many processors together via message transferring and also to extent easily. It should be noted that, the desired node is able to operate more than a process every time. A message is for a nodal communication as a logical unit is considered as a set of related information moved together. The message can be included as a instruction, data, synchronization or a interrupt signal. A transferring message system has

communication with external world by input or output messages. It is important external world have a meaningful understanding about the transferring message system. The relationship between processors and RAMs and also RAMs ' distributed manner to processors is shown in figure 8. [49]

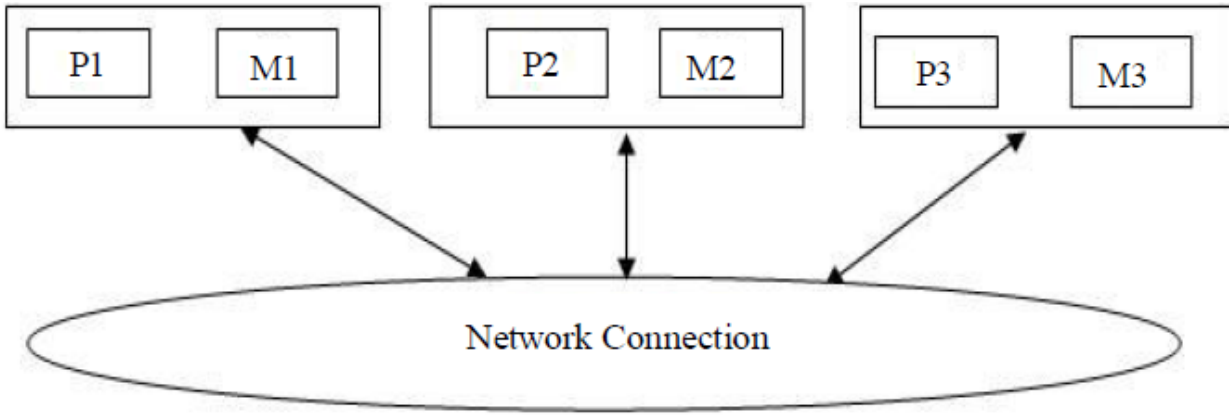


Figure 8. Distributed memory architecture

Block Diagram

The model block diagram is the CPUs' relationship to each other by bus and connect to RAMs by North Bridge. It is shown in figure 9.[47]

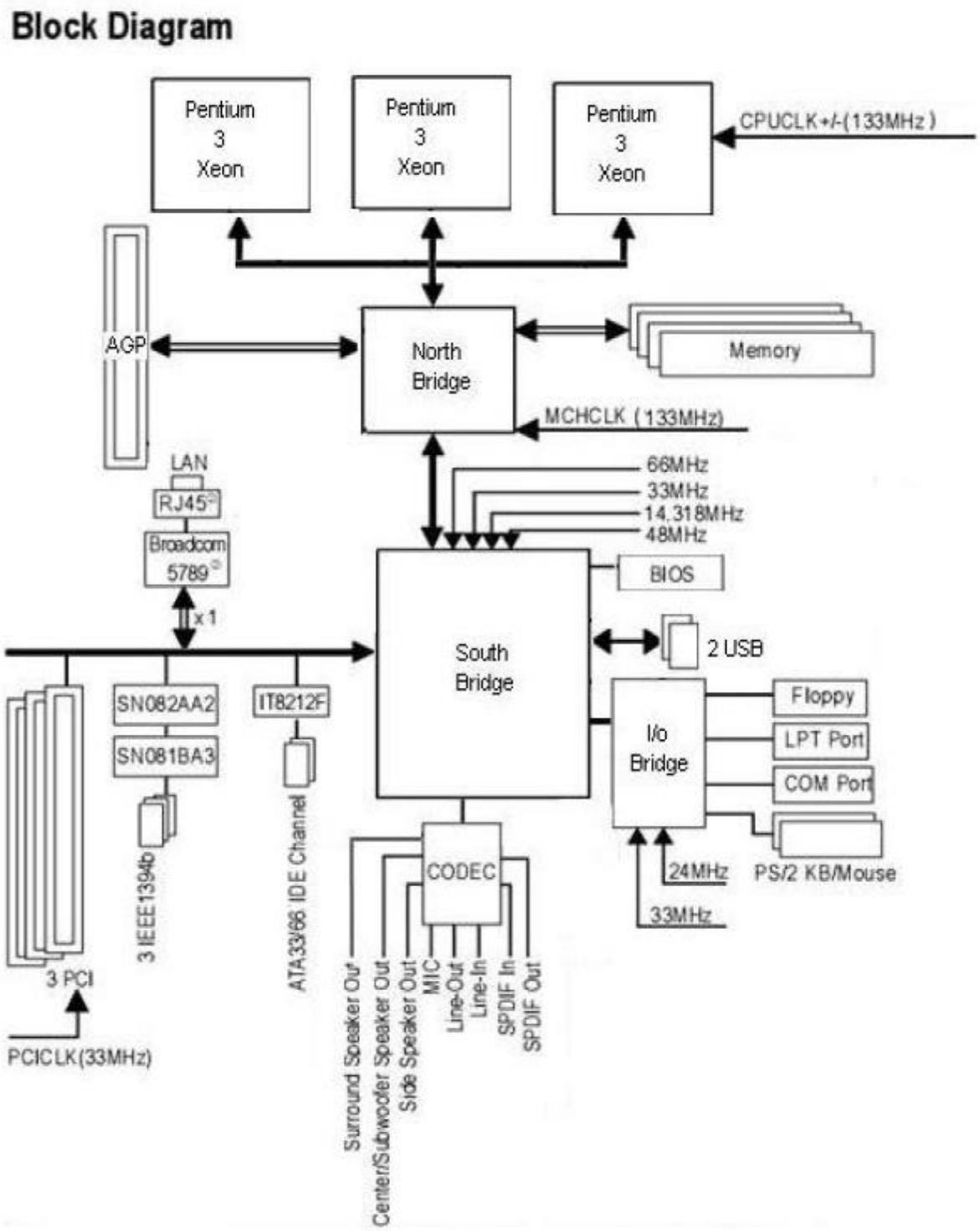


Figure 9. Block Diagram of the model

RAM in the model

Block Diagram of the model will be shown as distributed common memory. Each processor includes cache and uncached memory in our desired computer and it is connected to an intercommunication network. This kind of parallel computer is called as Non- Uniform Memory Access (NUMA). When each processor has own cache memory so it is necessary to keep their coherence between each processors. Therefore, today , "Cache Coherent Non-Uniform Memory Architecture" (CC-NUMA) is the best name for parallel computer with distributed common memory. CC-NUMA programming model has a common memory like as computer. In this section we try to review how the processors operate and solve a problem. A processor is able to show address after order to read (load the data from memory) where data is retrieved. The address divides in two parts by software: first is node number and second is the location address into node. If the node number was related to a processor which ordered to read, so data will be retrieved of its connected memory. Otherwise, the node number will be sent to a favor node memory in order to send a message for data retrieval and deliver to processor by intercommunication network. The relationship between the processor, RAM and cache is shown by figure 10.[49]

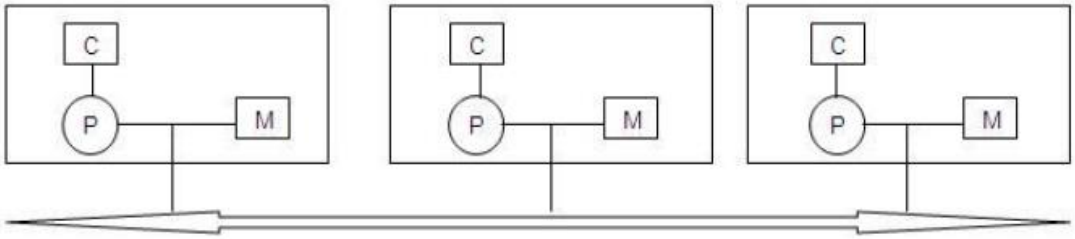


Figure 10. Memory Communications Architecture at CC-NUMA

Use of new generation CPUs at proposed model

For using new CPUs it is need to connect the provided Daughter board to CPUs board by soldered legs at the model and created a link between CPUs board and main motherboard. The CPU legs and Daughter board must be consistent each other and with the same number. Figure 11 is shown new processors board as imaginary.



Figure 11. New CPUs board

Power and temperature estimation at the model

The power and temperature are estimated in this section.

Estimate of calculating power at the model

The result of all calculating power for new motherboard is CPU 3with less than 1200W. It is possible to use Power ATX by Green 1235 B model for supplying power. The power can be used to add more CPU up to 12 processors of Pentium 3 Xeon.
According to calculating powers are mentioned in table 1, Core i7 will be supported up to CPU 7 by Power Green 1235B.

Solve the temperature problem at the model
The temperature and heat are the most important issues in computer and its components that the skilled users are familiar to it. Temperature is one of computer components' enemies, it does not occur in short time but gradually and in long time it causes to born, weak and char on components. CPU needs to consider and must not be more warm because more than 110o caused to prevent of its inner conductivity and disrupted completely, it stop temporarily, then made perfect disability. The CPU temperature is mentioned in table 2.

Table 2. Maximum Cpu temperature

In this model we have maximum Cpu temperature as following:

- Pentium II Xeon: 75° C
- Pentium III Xeon 600 MHz, 667 MHz and 733 MHz to 1 GHz: 55° C
- Pentium III Xeon 700 MHz: 65° C
- Pentium III Xeon 550 MHz: 68° C
- Pentium III Xeon 500 MHz: 75° C

The more professional way to decrease temperature is cooling with liquid nitrogen as called LN2. There is a tank included liquid nitrogen with high fixed temperature of -195o and the connectors to transfer nitrogen and a copper and cylinder dish used to keep it on processor.

Simulation Circuite
The model simulation by Proteus
In this article we discussed about the model simulation by Proteus. It is tried to use CPU and RAM for their operation and architecture and also to study and multiprocessor effect in PC motherboard. However there are some Proteus limitations in this simulation, but the code of 8051 is used for CPU which is able to connect with RAM and north bridge completely. The simulation is shown the full processing of addition process which is separated and displayed the relationship between CPUs and RAMs and also the north bridge interference. There is a program in this simulation like as Post program in PCs which investigated and examined the truth CPU and RAM operation in computer and also considered a perfect processing of addition process as we need . Figure 12 is shown that in this simulation first must be entered 3 numbers for addition operation , then add each numbers in CPU separately again and again , so the result of CPU 1 has sent to CPU 2 to add their results , and finally the last result will be gained by CPU 2 to CPU 3. The picture of simulation model in Proteus is mentioned according to figure 13.

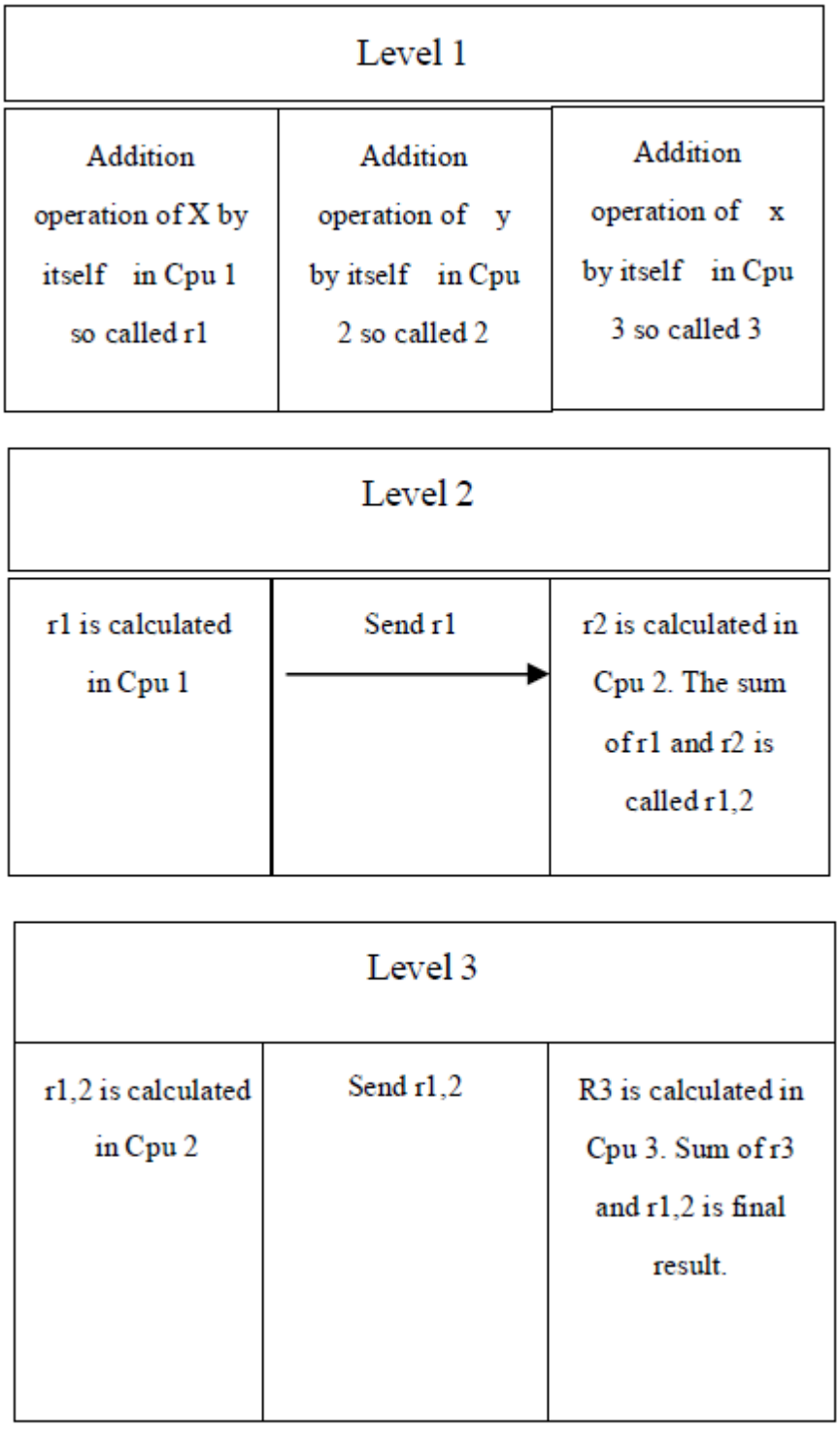


Figure 12. Processing levels in stimulation

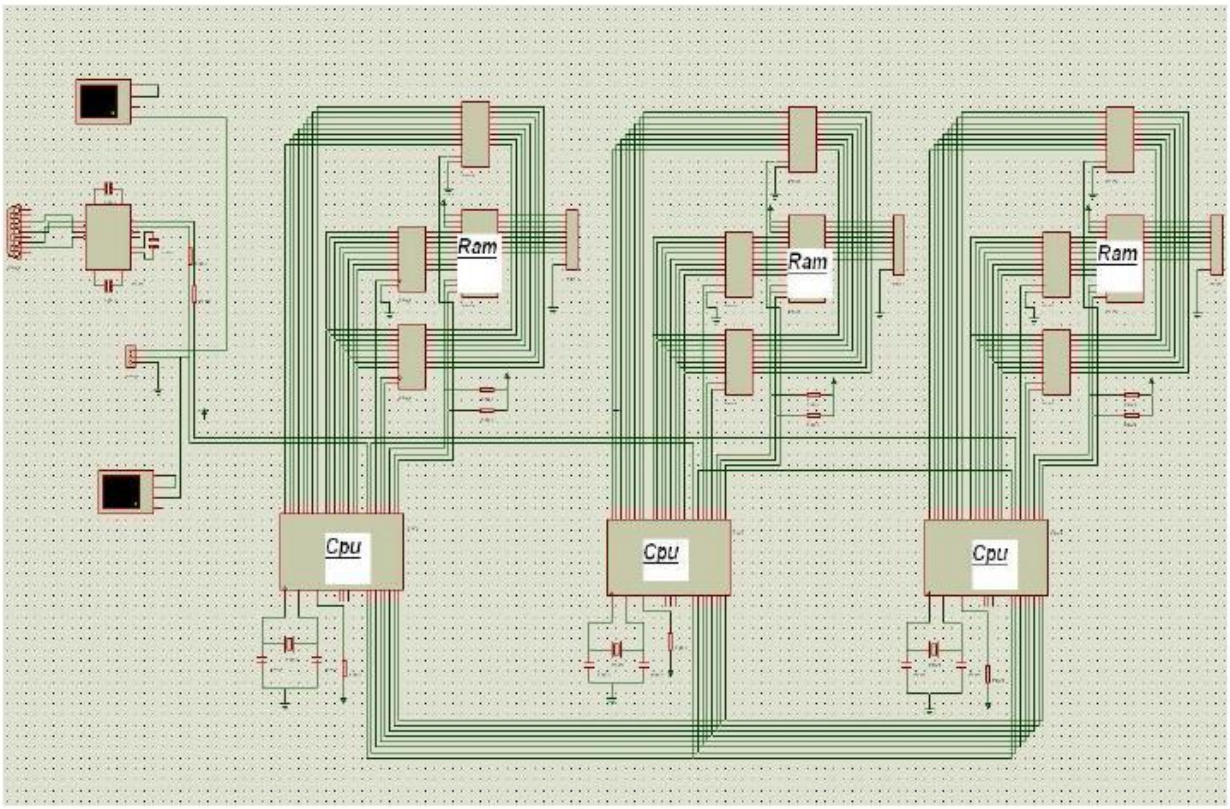


Figure 13. PC multiprocessor simulation in Proteus

During the plan, we gained to data are shown in table 3 and is shown in virtual terminal in figure 14.

Table 3. The Summarized data in the model

Time need for calculating		Total calculated numbers	Number of processors
0.2984	µs	3	1
0.2037	µs	3	2
0.1105	µs	3	3

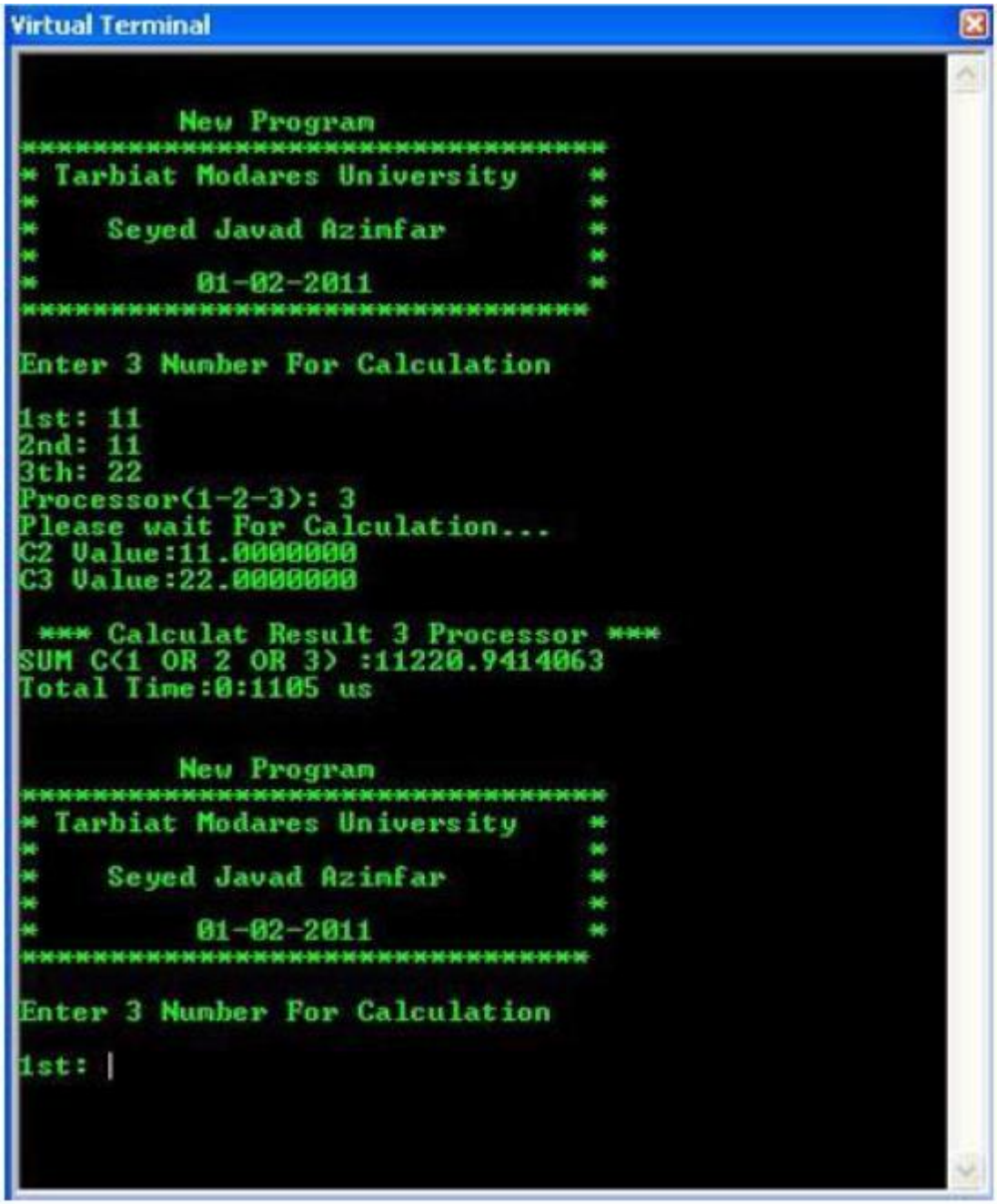


Figure 14. Sample of virtual terminal to receive input numbers

Conclusion

According to increase the computer speed, it was need to use parallelism in solving problem and computing which there was designed multiprocessor. Multiprocessor computers made as Super computer, then designed current servers. As we know, all components in proposed model are as motherboard. Our considered processor is Pentium 2/3 Xeon in this article, but the processor 8051 is used in Proteus because some limitations, its facility for connecting to CPU and RAM is like as a Pentium and it used for simulation. There is considered a board to install of

CPUs. The board is installed on main motherboard by Daughter board; however it created a wide place for CPUs installation but caused to empty and increased the maneuver on main board. The motherboard is called as Dual board because included two separated board; CPUs carrier and main board. Distributed architecture is as considered which each CPU have own RAM. This parallel computer is called as "Non-Uniform Memory Access (NUMA). When each processors
have own cache memory so must be coherent between each processors. Therefore, the best name for parallel computer with distributed common memory is "Cache Coherent Non-Uniform Memory Architecture" (CC-NUMA) .Also we learnt that the Symmetric Multi Processing (SMP) is considered in the model which operating system is able to operate on each free processor or all processors at the same time. The memory is shared between them. All processors can do the same acts. The all calculating power result for new motherboard is CPU 3with less than 1200W. It is possible to use Power ATX by Green 1235 B models for supplying power. The power can be used to add more CPU up to 12 Pentium 3 Xeon processors. The applied CPU is as Intel CPUs cooling and just keep cool by a usual Heat sink and fan. The more professional way to decrease temperature is cooling with liquid nitrogen as called LN2. For using new
CPUs it is need to connect the provided Daughter board to CPUs board by soldered legs at the model and created a link between CPUs board and main motherboard. The CPU legs and Daughter board must be consistent each other and with the same number. According to calculating powers are mentioned in table 1, Core i7 will be supported up to CPU 7 by Power Green 1235B. In this article we discussed about the model simulation by Proteus. It is tried to use CPU and RAM for their operation and architecture and also to study and multiprocessor effect in PC motherboard. According to new technology it is hoped to build such perfect and hardwired motherboard. The equation estimates the accelerated rate at the
model:[46]

$$S(n) \quad \frac{T(1)}{T(n)} \quad (1)$$

T(1) is sequence time of program on a processor
T(n) is sequence time of program on n processor
Addition of several numbers is good instance to estimate acceleration of this model. We consider the addition of numbers for n processor by multi cube computer. First, each processor receives a number for addition. One of the processors keeps sum of all numbers at the end of calculation. Image n is power of 2, so we can solve this problem by multi cube of n processor during Lon(n) level. Each level is included a sum and a messages between two processors are connected each other directly. So:[46]

$$T(n) \quad O(Log_n) \quad (2)$$

Because the problem is soluble during O(n) or a processor , so acceleration is :[46]

$$S(n) \quad O(\frac{n}{Log(n)}) \quad (3)$$

For n=3(3 processors) have:

[6] B. Bershad, T. Anderson, E. Lazowska, and H. Levy. Lightweight remote procedure call. ACM Transactions on Computer Systems, February 1990.
[7] B. Bershad, D. Redell, and J. Ellis. Fast mutual exclusion for uniprocessors. In Proceedings of the Fifth International Conference on Architecture Support for Programming Languages and Operating Systems, October 1992.
[8] B. Bershad, S. Savage, P. Pardyak, E. Sirer, M. Fiuczynski, D. Becker, S. Eggers, and C. Chambers. Extensibility, safety and performance in the SPIN operating system. In Proceedings of the Fifteenth ACM Symposium on Operating Systems Principles, December 1995.
[9] D. Black. Scheduling support for concurrency and parallelism in the mach operating system. In IEEE Computer, May 1990.
[10] R. Blumofe and C. Leiserson. Scheduling multithreaded computations by work stealing. Proceedings of the 35th Annual Symposium on Foundations of Computer Science, November 1994.
[11] H. Brice˜no. Decentralizing UNIX abstractions in the exokernel architecture. Master's thesis, Massachusetts Institute of Technology, February 1997.
[12] G. Candea. Flexible and efficient sharing of protected abstractions. Master's thesis, Massachusetts Institute of Technology, May 1998.
[13] D. Engler. The Exokernel operating system architecture. PhD thesis, Massachusetts Institute of Technology,1999.
[14] D. Engler and M. F. Kaashoek. DPF: fast, flexible message demultiplexing using dynamic code generation.In ACM Communication Architectures, Protocols, and Applications (SIGCOMM) 1996
[15] D. Engler, M. F. Kaashoek, and J. O'Toole Jr. Exokernel: an operating system architecture for application-level resource management. In Proceedings of the Fifteenth ACM Symposium on Operating Systems Principles, 1995.
[16] B. Ford, M. Hibler, J. Lepreau, P. Tullmann, G. Back, and S. Clawson. Microkernels meet recursive virtual machines. In Proc. of the Second Symposium on Operating Systems Design and Implementation,October 1996.
[17] B. Ford and S. Susarla. Cpu inheritance scheduling. In Proc. of the Second Symposium on Operating Systems Design and Implementation, October 1996.
[18] M. Greenwalk and D. Cheriton. The synergy between non-blocking synchronization and operating system structure. Proceedings of the Second Symposium on Operating Systems Design and Implementation, 1996.
[19] M. Herlihy. A methodology for implementing highly concurrent data structures. ACM Transactions on Programming Languages and Systems, November 1993.
[20] Intel Corporation. Intel 82093AA I/O Advanced Programmable Interrupt Controller (IOAPIC) Specification.May 1996
[21] Intel Corporation. Intel Pentium Pro Developer's Manual. Volume 1: Specifications. January 1996.
[22] Intel Corporation. Intel Pentium Pro Developer's Manual. Volume 3: Operating System Writer's Guide.January 1999.
[23] M. F. Kaashoek, D. Engler, G. Ganger, H. Brice˜no, R. Hunt, D. Mazi`eres, T. Pinckney, R. Grimm, J. Jannotti, and K. Mackenzie. Application performance and flexibility on exokernel systems. In Proceedings of the Sixteenth ACM Symposium on Operating Systems Principles, 1997.
[24] M. F. Kaashoek, D. Engler, G. Ganger, and D. Wallach. Server operating systems. In Proceedings of the 1996 SIGOPS European Workshop,September 1996.
[25] H. Massalin and C. Pu. A lock-free multiprocessor os kernel. Technical Report 005-91, Columbia University Computer Science Department, 1991.
[26] D. Mazieres and M. F. Kaashoek. Secure applications need flexible operating systems. In Proc. of the Sixth Workshop on Hot Topics in Operating Systems, 1996.
[27] J. Ousterhout. Scheduling techniques for concurrent systems. In Proc. of 3rd International Conference on Distributed Computing Systems, 1982.
[28] V. Pai, P. Druschel, and W. Zwaenepoel. IO-Lite: A unified i/o buffering and caching system. Proceedings of the Third Symposium on Operating Systems Design and Implementation, February 1999.
[29] T. Pinckney III. Operating system extensibility through event capture. Master's thesis, Massachusetts Institute of Technology, February 1997.

[30] M. Seltzer, Y. Endo, C. Small, and K. Smith. Dealing with disaster: Surviving misbehaved kernel extensions. In Proc. of the Second Symposium on Operating Systems Design and Implementation,October1996.
[31] R. Wisniewski, L. Kontothanassis, and M. Scott. High performance synchronization algorithms for multiprogrammed multiprocessor. Proceedings of the 5th Symposium on Principles and Practice of Parallel Programming, 1995
[32] T. E. Anderson. The performance of spin lock alternatives for sharedmoney multiprocessor. IEEE Transactions on Parallel and Distributed Systems, 1990.
[33] L. Hammond, B. D. Carlstrom, V. Wong, M. Chen, C. Kozyrakis, and K. Olukotun, "Transactional coherence and consistency: simplifying parallel hardware and software," IEEE Micro, Vol. 24, No. 6, Nov.– Dec. 2004
[34] L. Hammond, B. Hubbert, M. Siu, M. Prabhu, M. Chen, and K. Olukotun, "The Stanford Hydra CMP," IEEE Micro., Vol. 20, No. 2, Mar.– Apr. 2000
[35] V. Krishnan and J. Torrellas, "A chip multiprocessor architecture with speculative multithreading," IEEE Trans. Comput., Vol. 48, No. 9, Sept. .
[36] G. Sohi, S. Breach, and T. Vijaykumar, "Multiscalar processors," in Proc. 22nd Annual Int. Symp.ComputerArchitecture, Santa Margherita Ligure, Italy, June 1995.
[37] J. G. Steffan and T. Mowry, "The potential for using thread-level data speculation to facilitate automatic parallelization," in Proc. 4th Int. Symp. High-Performance Computer Architecture (HPCA-4), Las Vegas, NV, Feb. 1998.
[38] J. F.Martinez and J. Torrellas, "Speculative synchronization: applying thread-level speculation to explicitly parallel applications," in Proc. 10th Int. Conf. Architectural Support for Programming Languages and Operating Systems (ASPLOS-X), San Jose, CA, Oct. 2002.
[39] A.Zhai, C. B. Colohan, J. G. Steffan, andT.C.Mowry, "Compiler optimization of scalar value communication between speculative threads," in Proc. 10th Int. Conf. Architectural Support for Programming Languages and Operating Systems (ASPLOS-X), San Jose, CA, Oct. 2002.
[40] T. Sherwood and B. Calder, "Time varying behavior of programs," Dept. of Computer Science and Eng., UCSD, Tech. Rep. No. CS99-630, Aug. 1999.
[41] M.K. Prabhu and K. Olukotun, "Exposing speculative thread parallelism in SPEC2000," in Proc. Principles and Practices of Parallel Programming 2005 (PPoPP 05), Chicago, IL, June 2005.
[42] T. Wilkinson, Kaffe Virtual Machine, http://kaffe.org, 1997– 2002.
[43] M. K. Chen and K. Olukotun, "The Jrpm system for dynamically parallelizing Java programs," in Proc. 30th Int. Symp. Computer Architecture (ISCA-30), San Diego, CA, June 2003.
[44] S. Woo, M. Ohara, E. Torrie, J. P. Singh, and A. Gupta, "The SPLASH2 programs: characterization and methodological considerations," in Proc. 22nd Int. Symp. Computer Architecture (ISCA-22), Santa Margherita Ligure, Italy, June 1995.
[45] D. O'Hallaron, "Spark98: sparse matrix kernels for shared memory and message passing systems," School of Computer Science, Carnegie Mellon University, Tech. Rep. CMUCS 97-178, Oct. 1997. IMPROVING LATENCY USING MANUAL PARALLEL PROGRAMMING 139 Books:
[46] J. R. Larus and R. Rajwar, Transactional Memory. San Rafael, CA: Morgan & Claypool Publishers, 2006.
[47] S.Mueller, "Upgrading And Repairing PCs",19th Edition,Que,December 2009
[48] V.Rajaraman, Si Siva Ram Mourti- translated by Dr. Sepidnam, The architecture & Programming of Parallel Computers, , Computer Sciences Publishing Co. Autumn 2005.
[49] Hesham AL-Raviti, Mostafa Abdulbar- translated by Dr. Ali Naseri, Mohammad Nezam Abadi, " Advanced Computer Architecture & Parallel Processing", , Imam Hossain(AS) University Publishing Co2005.
[50] Majid Naderi," Advanced Computer System Architecture & Design & Parallel Processing, Iran Science and Industry University Publishing Co 1999.