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A New Algorithm for Analog Background Calibration in High Speed Analog to Digital Convertors

Kuresh Ghanbari[1], Milad Abtin[2]

1. *Islamic Azad University, Masjed Soleiman branch, Masjed Soleiman, Iran*
2. *Islamic Azad University, Masjed Soleiman branch, Masjed Soleiman, Iran*

Abstract

In this paper a new algorithm for analog background calibration in pipeline ADCs is presented. The algorithm is based on error detection and separation of the stages without requiring the reference voltage. The error detection is digital based and correction is analog based and execute on MDAC of each stage. Simulations results for calibrating a 12-bit pipeline ADC demonstrated that with this method, ENOB can be corrected from 6.82 to 11.72 bits. The algorithm can be used in all kinds of pipeline ADCs.

Keywords: algorithm, pipeline ADC, analog background calibration, error detection.

Introduction

Pipeline ADCs have a lot of advantages compared to the other ADC architectures. Because they can simultaneously realize high speed and high precision [1]. In pipeline ADCs usually errors will occur in the Sub-ADC and MDAC block [2]. The main source of error in the Sub-ADC block is offset error and gain error [3]-[4].
Using Redundant Signed-digit Decoding (RSD) method will reduce offset error and sometimes eliminates it [5], but the effect of MDAC's errors will remain in the output.

Thus, calibration for ADCs with high resolution is undeniable and both analog and digital calibration methods can be used [6]-[7].
In analog calibration method, the circuits must be corrected in converter blocks. Sometimes in analog calibration, an extra ADC channel with analog calibration circuits has been used [8]. Multi-bit switched MDAC capacitors are other analog calibration techniques [9].
In digital calibration method the error can be determined regarding output and will be applied on the final output [10]. Also some statically background calibration techniques have been used to digitally trim the input-referred offset voltage of comparators [11]. Linearity error due to capacitor mismatches in pipelined

ADCs is unquestionable. In improving this defect digital background calibration technique would be practical [3].
In this paper in order to correct the MDAC gain error an analog background calibration technique has been used. This algorithm is operating without any access to the output bit of any stage; the stages are not able to separate the error. Usually, previous background calibration techniques used one reference voltage for recognized the error. The most important defect of this method is that all of the inputs for calibration cannot be used and only some inputs (about 42% that this average will be increased) are used for calibration.
Here, in this paper pipeline structure and its features will discuss in part II. In part III proposed error detection algorithm will be presented. Part IV describes calibration circuit. In part V shows and discusses simulation result. Conclusion and suggestions will present in part VI and VII respectively.

Pipeline Structure

Fig. 1 shows Pipeline ADC structure which is used in this article. The analog to digital converter has 12-bit resolution. this converter is consists of nine stages, the first stage has 3 bits, second stage, 1 +2 bits (also 2 bits with one level added and the difference of it with 2.5 bits is that 4 comparators is used) the third to the eighth stages are 1.5 bit and the ninth stage is 2-bit flash ADC. The gain in the first and second stages is equal to 4 and for 1.5 bits stages equal to 2.

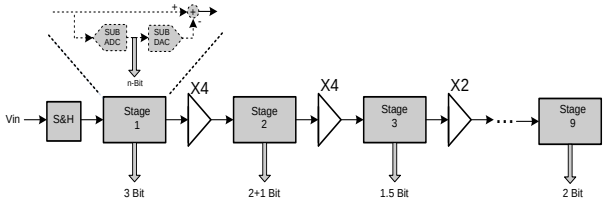


Fig.1. Block Diagram of 12-Bit Pipeline ADC

Error Detection Algorithm

Calibration is done in two parts: error detection and error correction. Gain calibration in analog to digital converters in most significant bits is so important, so the first 5 bits that included the first two stages are calibrated. Errors in two first stages have more affect on final outputs although error in next stages has less importance.
Conventional block for a single stage has shown in Fig. 2. n_i is each stage bits, b_i is number of bits in next stage, R_i is residue of each stage and V_r is reference voltage. Calculations for each of these stages are performed as follow:

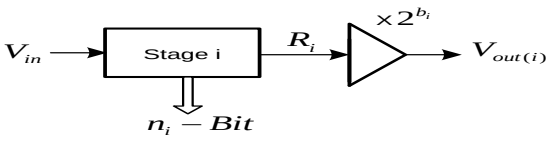


Fig.2. Block Diagram of Stage i

In the normal state assume that: $b_i = n_i$

$$R_{i(\max)} = \frac{V_r}{2^{n_i}} \quad (1)$$

$$V_{out(i)} = R_i \times 2^{b_i} \rightarrow V_{out(i\ \max)} = R_{i(\max)} \times 2^{b_i} \quad (2)$$

While K_i is error gain in each stage, $error_i$ is each stage error and regarding closed loop gain error:

$$V_{out(i\ \max)} = R_{i(\max)} \times 2^{b_i}(1+K_i)$$

$$= \frac{V_r}{2^{n_i}} 2^{b_i} + K_i \frac{V_r}{2^{n_i}} 2^{b_i} \rightarrow error_i = K_i V_r \times 2^{(b_i - n_i)} \quad (3)$$

$$error_i \langle \frac{1}{2} LSB_{(N-\sum_{j=1}^{i} n_j)}$$

$$V_{Full-Scale\ Input\ of\ Stage(i+1)} = 2V_r \times 2^{(b_i - n_i)} \quad (4)$$

$$LSB_{(N-\sum_{j=1}^{i} n_j)} = \frac{2V_r \times 2^{(b_i - n_i)}}{2^{(N-\Sigma_{j=1}^{i} n_j)}} \quad (5)$$

$$error_i \langle \frac{1}{2} LSB_{(N-\sum_{j=1}^{i} n_j)} = \frac{1}{2} \frac{2V_r \times 2^{(b_i - n_i)}}{2^{(N-\Sigma_{j=1}^{i} n_j)}}$$

$$K_i V_r \times 2^{(b_i - n_i)} \langle \frac{1}{2} \frac{2V_r \times 2^{(b_i - n_i)}}{2^{(N-\Sigma_{j=1}^{i} n_j)}} \quad (6)$$

$$\Rightarrow K_i \langle \frac{1}{2^{(N-\Sigma_{j=1}^{i} n_j)}}$$

So, if the number of bits in a stage is more, the closed loop will be authorized to the larger percentage of error.

Since:

$$R_i = V_{in} - V_{DAC} \quad (7)$$

So with increasing input and stabilizing V_{DAC}, R_i will increase. This is the time to change the V_{DAC}. so If the second stage have an error, and the output of first stage is 3 bits, near the points that the first 3 bits change the situation we can see the much errors. Now if second stage gain has error, this status becomes clear while the fourth and fifth bits changed the positions.

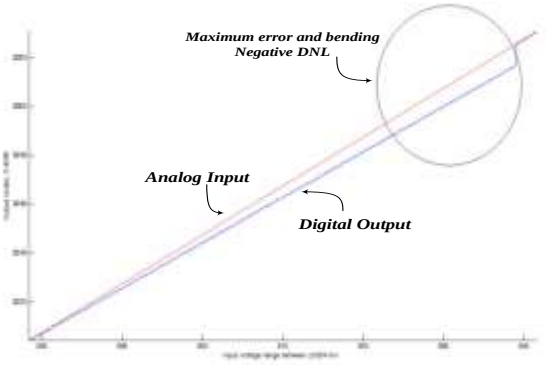
Proposed error calibration idea comes from these errors situations. As shown in Fig. 3, as input error is increased finally the graph will have breakage and in average in some outputs errors will occurred. Considering to the range of input that located in this situation, it will be realized that the converter has an error or not? We named this situation "error boundaries".

Residue = (Actual ADC output – Ideal ADC output) (8)

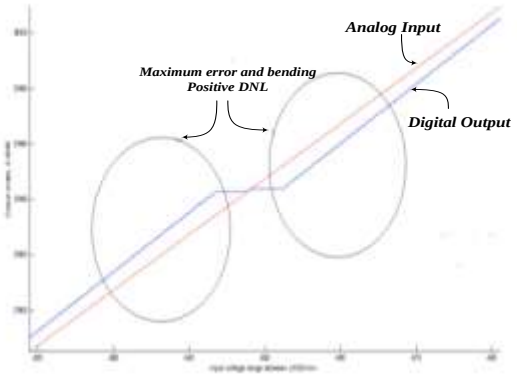
In order to simplify calculations, assume the input voltage in range of -1024mV to +1024mV, so V_{LSB} will be calculated as follow:

$$V_{LSB} = \frac{2048}{2^{12}} = 0.5mV \quad (9)$$

This converter has been allowed having LSB error. Residue calculation and comparison with V_{LSB} will show the situation of system error for any stage.



(a)



(b)

Fig.3. Output curve after (a) decreasing gain error (b) increasing gain error

Calibration Circuits

As shown in Fig. 4, input is applied to the ADC. These inputs are stored in one Latch. The 12-bit of the input is generated by both real ADC and ideal ADC. Gain controller recognizes that the value is in error range or not, and then if no error were detected next input value would be examined. If any error range were recognized, input value would be fed to an ADC with low speed and very low error (assumed as ideal ADC). At this step output bits of actual ADC and ideal are being compared and calibration will be actuated if LSB is more than 1. Also real ADC output is stored in another Latch. Correct digital 12-bit attain from input by ideal ADC. Now the real ADC and ideal ADC output bits are compared with each other. Real ADC is allowed to make LSB error. Low bits of both ADCs neither are nor compared. To simplify the circuit, assume that really ADC has 6-bit accuracy. So that 6 bits are not rewarding to compare the two converters. Thus, Comparison is done between the seventh to the eleventh bit of both ADCs. This is done by a 5 bits digital comparator circuit (which has three outputs) with three different output states. If these 3 outputs are the same, it means that the converter requires no calibration. If there are differences between the states of outputs then gain controller will make decision for increasing or decreasing of gains for first and second stages depending on outputs of 3 bit comparator.

Error correction

After detection of error and the stage that makes error, the gain should be corrected. Correction will be done by variation of the amount of a tuning capacitor C_f in the MADC circuit as shown in Fig. 5 and Fig. 6. It means by changing the value of the capacitor, its gain in the stage is getting more or less. This is done by connecting a capacitor in parallel with the capacitor C_f. Fig. 5 and Fig. 6 show MDAC blocks first and second stages with variable feedback capacitor.

Calibration Speed

As discussed before, the calibration is naturally possible and all inputs are not used for error detection. In a 12-bit converter, there are 4096 codes; it means the output will have a code in the range of 00000000000 to 111111111111. By using only 5 bits, if the digital input code for example is in the range of 000000000000 to 000000011111, they will be used for calibration. So, 32 states of 4096 will used. If other limitations for 5 bits are considered, these codes will be increased to 736 that are 18% of whole codes. Therefore probability of having an input that can be used to calibrate the first stage is 18%. If the gain of the first stage increases, a large error will be occurred in following codes:

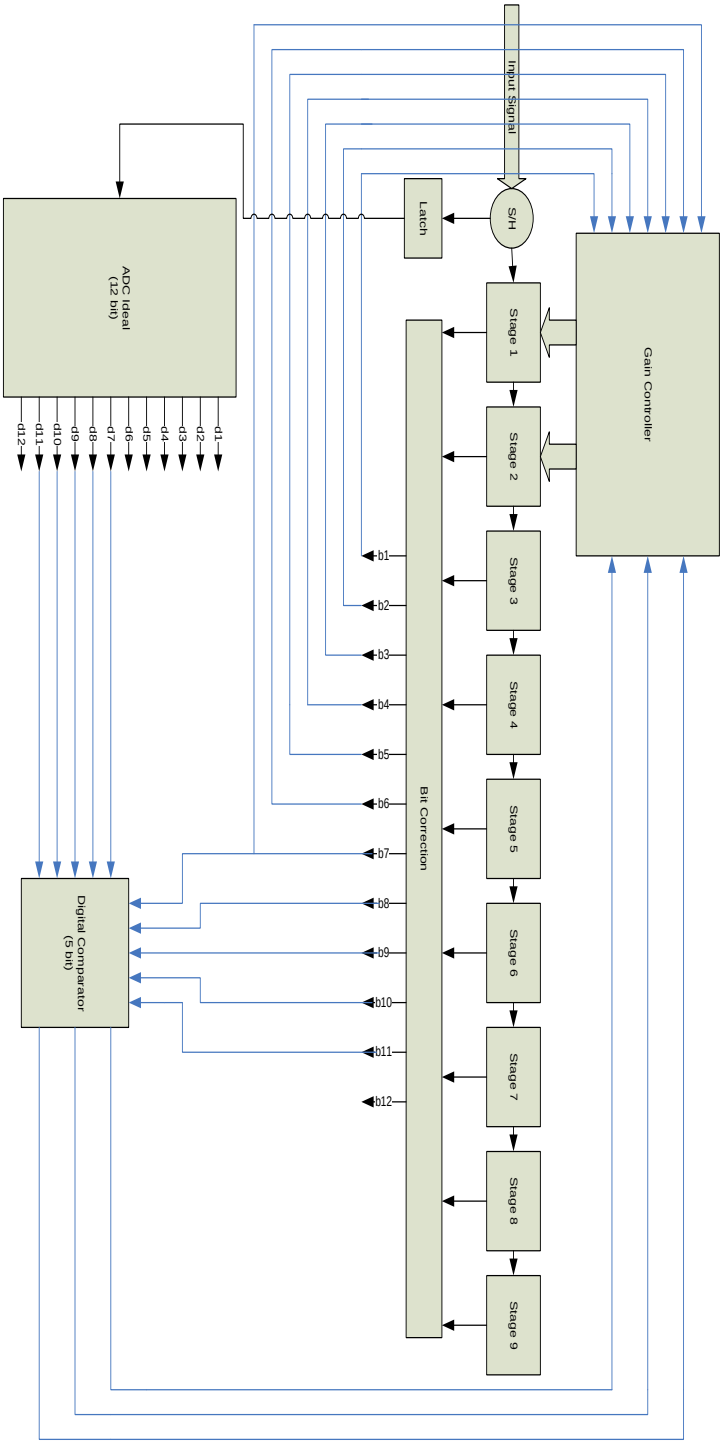


Fig.4. Total Schematic of ADC and Calibration Block

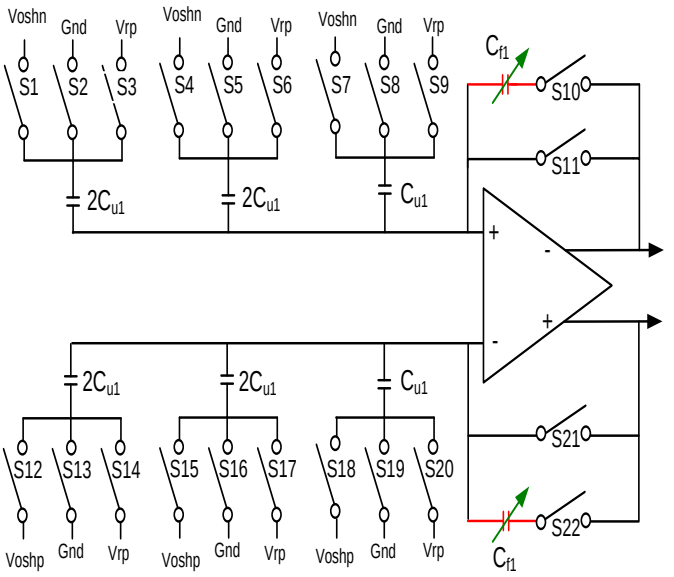


Fig.5. 3-bit MDAC block which changing in C_{f1} will change first stage

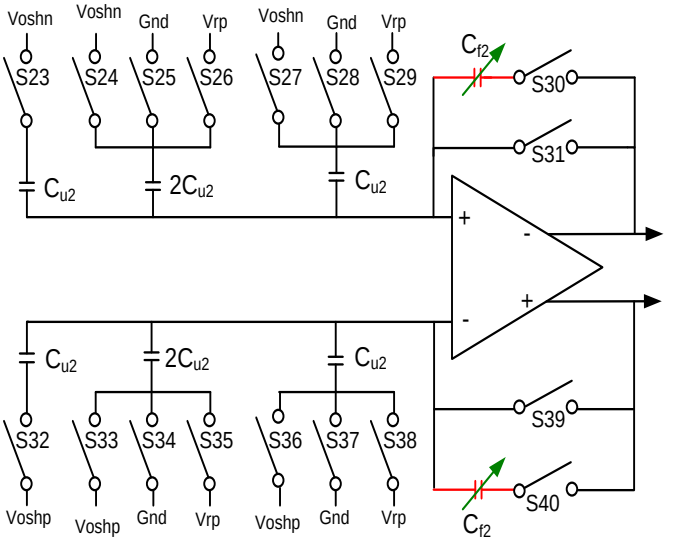


Fig.6. 2.5-bit MDAC block which changing in C_{f2} will change second stage gain

Table I: Codes in which more errors have occurred when increasing the first stage gain while residue > V_{LSB}

B_1	B_2	B_3	B_4	B_5	B_6	B_7	B_8	B_9	B_{10}	B_{11}	B_{12}
0	0	0	0	0	0	0	0	0	0	0	0
0	0	1	0	0	0	0	0	0	0	0	0

0	1	0	0	0	0	0	0	0	0	0	0
0	1	1	0	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	0	0	0	0	0
1	0	1	0	0	0	0	0	0	0	0	0
1	1	0	0	0	0	0	0	0	0	0	0
1	1	1	0	0	0	0	0	0	0	0	0

Table II: Codes in which more errors have occurred when increasing the first stage gain while residue < V_{LSB}

B 1	B 2	B 3	B 4	B 5	B 6	B 7	B 8	B 9	B 10	B 11	B 12
0	0	0	1	1	1	1	1	1	1	1	1
0	0	1	0	1	1	1	1	1	1	1	1
0	0	1	1	1	1	1	1	1	1	1	1
0	1	0	0	1	1	1	1	1	1	1	1
0	1	0	1	1	1	1	1	1	1	1	1
0	1	1	0	1	1	1	1	1	1	1	1
0	1	1	1	1	1	1	1	1	1	1	1
1	0	0	0	1	1	1	1	1	1	1	1
1	0	0	1	1	1	1	1	1	1	1	1
1	0	1	0	1	1	1	1	1	1	1	1
1	0	1	1	1	1	1	1	1	1	1	1
1	1	0	0	1	1	1	1	1	1	1	1
1	1	0	1	1	1	1	1	1	1	1	1
1	1	1	0	1	1	1	1	1	1	1	1
1	1	1	1	1	1	1	1	1	1	1	1

As can seen, the first stage error has occurred near 23 codes.

$$A = 2^{12} = 4096 \qquad (10)$$

$$B_1 = (8 \times 32) + (15 \times 32) = 736 \qquad (11)$$

$$P_1 = \frac{736}{4096} \times 100 \approx \%18 \qquad (12)$$

If this method is used for the second stages, the error has occurred near 31 codes.

$$B_2 = (16 \times 32) + (15 \times 32) = 992 \qquad (13)$$

$$P_2 = \frac{992}{4096} \times 100 \approx \%24 \qquad (14)$$

Thus, the probability that an input can be used in calibrating in the second stage is 24%. The chances of an ADC converter input that can be used in calibration, is 42%. If the error is identical in each stage, second stage can be calibrated earlier. The speed of calibration depends on several factors:

A) Error rate in each stage: according to the increase or decrease gradual gain and step by step. If the stages error rate is more, more input samples will be needed to detect error. And more time on correcting errors will be spent.

B) Step variations of feedback capacitor: With increasing amount of steps, the accuracy will be increased but the speed reduces and vice versa.
C) Speed of ideal ADC: The ideality makes accuracy better and enhances the speed.

Simulation Results

An example of 0.5 MHz sinusoidal input voltage is investigated while sampling frequency is 4.094 MHz. Two experiments are executed before and after calibration with a gain variation of 0.06 for first stage and 0.07 for second stage. Before calibration ENOB was 6.82bits and SNDR was -42.83db. Then after calibration ENOB became 11.72bits and SNDR became -72.32db. Also three experiments were done by MATLAB and the results are shown in table III.

Table III: Results in three tests, before and after calibration

	First Test		Second Test		Third Test	
	Before	After	Before	After	Before	After
SNDR	38.73	72.17	42.83	72.32	44.42	72.32
SNR	40.45	72.22	44.47	72.37	46.35	72.37
THD	43.60	91.38	47.85	91.62	48.88	91.62
SFDR	46.18	96.08	51.79	95.73	51.79	95.73
ENOB	6.14	11.70	6.82	11.72	7.09	11.72

Conclusion

In this article a specific method is presented for analog calibration of a pipeline ADC. The ADC will be calibrated in a few times by means of 2 stage adjustment. A high accuracy ADC is needed for this background calibration. Less complexity of the analog circuit in this ADC causes low power consumption of whole circuit. Because digitals circuits that is used for recognizing errors are simple circuits and have low power consumption. Also reference voltage is not necessary for this ADC which is applied in all background techniques. Convergence time depends on the calibration to the ADC. As the conversion speed is increased, error detection rate will be increased.
Calibration presented in background analog form. Advantages of this type of calibration are low power consumption and low volume of the used circuits. Also the convergence rate is acceptable during the calibration value.

Suggestions

The method will also be expanded for other pipeline converters. By simulating any pipeline and getting expended that more errors happened in them, a calibration algorithm will be resulted.
This converter has 12 bit outputs. We used the eighth to eleventh to know that the input can be used for calibration. This inputs involved 42% of the total inputs. If we choose the larger of this breadth it means instead of the eighth to eleventh bits, consider seventh to eleventh bit, we can use more inputs for calibration. It can speed up the calibration but the consumed power will increased in calibration circuit.

Also the error of one stage is not much and sometimes if this samples been used, there are less than 1LSB and cannot be realized that the convertor need calibration or not.

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