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Data Analysis of Digital Testing for a NAND Gate: Electrical and Business Approaches

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Abstract

The purpose of this paper is to describe the testing of a digital SN74HC00N NAND gate. The tests were derived from the part's datasheet and were implemented not only to confirm the functionality of the device but also to see how well the chip can function when tested multiple times and with different equipment. The testing of each gate allowed for a better understanding of the device's performance as well as the accuracy and performance of the testing instruments.

Keywords: Digital Test, Integrated Circuit, Nand Gate, Voh, Vol, Cpk, GRR, Busines.

Introduction:

Testing a device has many usages, a primary one being to affirm the functionality of the product before it is shipped to the customer.This arises the financial consumption development for companies as well as IC production trade (Çiftçioğlu and Almasifard, 2015; Almasifard and Saeedi, 2017; Almasifard and Khorasani 2017). Another important usage is finding flaws in design or manufacturing so that they may be fixed and prevented from appearing in all future products. Testing in total reveals many important aspects of the device under test (DUT) and also the testing equipment. With every passed and failed test, a device may be redesigned to be faster and more robust, and testing equipment and programs can likewise be improved to be quicker and more accurate.

However, the fundamental architecture of the digital pattern generator and its inherent limitations have not changed (Aslanian, 2012).Testing in the industry is done on very advanced instruments known as automated test equipment (ATE). These ATE's can force and measure voltages with number sense and measure lines (SMU) with high degrees of accuracy. For example, current leakages can be measured down to fractions of 1μA with this technology. The level of Digital Signal Processing contained within vehicles continues to grow significantly (Boyraz et al, 2012).

Final Tests are done to confirm the performance of the device by testing its corners. This is done for products to be shipped, to send only devices that satisfy the datasheet (and even over-satisfy it), and also for customer returns. Logic design of digital devices is a very important part of the Computer Science (Adamsky, 2011).

These tests are usually meant to test corner-specs and be as fast as possible- generally 100ms or less. Characteristic Tests are done to completely test the chip at a range of specs and stress it to validate the design of the chip. This test can be done at probe level before the silicon is packaged, while final testing can happen after packaging.

Business of Testing

While testing is extremely essential to maintain customer satisfaction and safety (Khorasani, 2014; Ghanbari et al, 2012), it is actually the most expensive piece of a device's lifespan. Since silicon die can be made smaller and smaller while the cost of silicon wafers remains relatively constant, this means manufacturing a device is significantly cheaper than testing it. While Fabs must use large funds to fabricate devices in a dust and debris free environment, testing also involves large costs with expensive ATEs and handlers. Additionally, the human element of testing is very costly. Where automated machines can fabricate devices from silicon, people must be used to place devices in testers and handlers, create software, and implement the software.As it clearly stated, efficient cost management of this testing absolutely essential (Khorasani and Almasifard, 2017).

Another expensive feature of testing is the need for a maximum of working parts shipped to a customer (Torabzadeh and Memarian, 2012). To achieve this, guard bands are placed on testing limits (Aslanian, 2012). Testing limits are the boundaries that determine a working part that meets the datasheet's specs from a malfunctioning part. Malfunctioning parts are never sold. Parts that perform slightly under spec are sometimes sold at a lower price. For example, resistors that do not meet 5% tolerance specs are sold as 10% resistors. Guard bands are buffers that make sure a part that performs close to a limit is thrown away, or at least not grouped with the lot of acceptable, working devices. As a result, only robust parts are shipped to a customer. However, this results in high yield loss which costs a company lots of money. A careful balance of guard bands that are not too large to allow for good parts being shipped without too high of a yield loss must be created.

Gauge Reputability and Reproducibility

Gauge Reputability and Reproducibility (GRR) is a measurement made concerning the noise of the instruments used to test a device and provides a certain confidence in a test. All instruments carry a level of inaccuracy, and this changes with the user, temperature, and a number of other variables. By measuring the standard of deviation of testing a chip numerous times (from 100 to 1000) times, and by measuring the standard of deviation of a test with different users and different versions of a given instrument, a sigma-repeatability and sigma-reproducibility can be derived respectively. These two measurements can then be used to find a Cp-measured (explained later). The higher this value, the lower the variance or noise in the instrument. Then, GRR is derived by in the following equation:

$$Cp_{measured} = \frac{USL - LSL}{6 * \sqrt{\sigma^2_{repeat} + \sigma^2_{reprod}}} \quad , \quad GRR\ (\%) = \frac{100}{Cp_{measured}} \qquad \textbf{Equation 1}$$

A low GRR, usually 1%, is optimal. This means that when a device past a test, a company can be confident that the test actually is a working one. However, a low GRR (of 20 to 50%) signifies that there is high noise in the instrument and a passing-chip might actually be malfunctioning or not up-to-spec in reality.

CP and CPK

'Cp' stands for Process Capability and 'Cpk' stand for Process Capability Index. CP is a ratio of the variability the customer is willing to accept over the variability a factory can produce. When a customer accepts a wide range of parts (where USL- upper spec limit- and LSL- lower spec limit- are far apart), this means profit is high and business is good. A disparity between what the customer wants and what the factory can provide exists, business suffers. A high CP implies a very narrow distribution where most parts are close to a mean measurement with little deviation.

CPK determines where a distribution of a part's measurement data exists within a customer's limits. When CPK is high, this means that the distribution is centered at the mean. However, due to problems with manufacturing or testing, a distribution can be centered near one of the customer's limits. This means that many of the parts do not meet spec and must be thrown away, which is a loss of money for the company. Many corrections in design, production, and testing must be made to make CP and CPK as high as possible. Usually, numbers above 2 and 1.5 respectively are targeted. With high CP and CPK, a tight distribution of measurements exists comfortably far from the customer's limits, and near 100% of the devices manufactured can be sold and provide a profit. This is the best possible outcome for a business. With lower CP and CPK values, a customer is negotiated with so he will consent to accept a greater range of parts, or guard bands can be widened while raising the price of the part.

Device and Equipment

The device chosen for this project was the SN74HC00N NAND gate for its simplicity. Because testing did not need to be too extensive to test the 6 parameters on the datasheet, the focus could be placed on creating complex tests that contained both accuracy and precision instead of wrestling with understanding the complexities of the device.

The chosen equipment was two NI MyDaqs that function off of the LabView programming languages, an NI Virtual-Bench, and a Keithley 2400 with a LabView interface. The MyDaq was chosen because of its portability, and facilitation of relatively simple code that we could write ourselves. The Keithley was used to provide accurate current measurements (less than 1µA) where the MyDaq was not able to. Rezaie and Stoneham focused on MyDaq code and Boit took it upon himself to fully understand and implement the Keithley SMU.

Tests

The implemented tests were derived from the datasheet: VOH and VOL The first 2 were tested on the MyDaq. Each was performed 100 times to derive a robust distribution and make useful deductions about CP and CPK. The last 2 were tested on the Keithley 2400. COUNTY is functionality was not included on the datasheet but is standard tests used in industry to further demonstrate the functionality of the device as a whole.

County Code

In order to test the SN74HC00N chip with the MyDaq, NI LabView code was used. Jmp software was used for data analysis. For the COUNTY test, we needed to acquire data (voltage) from MyDaq and then send the voltage to a comparator to check if the measured voltage is within range- i.e a usable voltage drop is recorded. This drop is expected to be 0.7 V. The limits of 0.2 and 0.9 were chosen accordingly. As can be seen in the below figure, our code consists of DAQ Assistant that acquires data to then feed into a comparator. If the output of the comparator is a logic high, the data is within range and the test passes. Otherwise, the test fails. Lastly, the pass or fail is written to an Excel file.

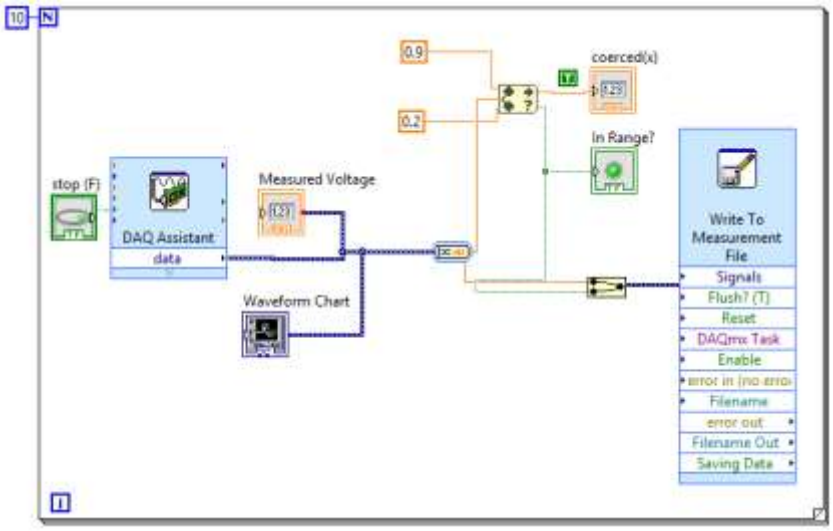


Figure 5: CONTY Code

A snippet of the results are shown below for negative and positive CONTY tests.

	Pin1 (volts)	Pin2 (volts)	Pin3 (volts)	Pin4 (volts)	Pin5 (volts)	Pin6 (volts)	Pin9 (volts)	Pin10 (volts)	Pin11 (volts)	Pin12 (volts)	Pin13 (volts)	Pin14 (volts)
2	0.731258	0.73191	0.529479	0.732236	0.734191	0.592392	0.730932	0.72865	0.601519	0.732887	0.729302	0.602171
3	0.730606	0.731258	0.580005	0.730932	0.736799	0.604127	0.730932	0.661499	0.602171	0.715611	0.730932	0.601193
4	0.732561	0.731584	0.604453	0.732887	0.732561	0.605105	0.730932	0.731584	0.602171	0.732561	0.727346	0.581309
5	0.734517	0.73191	0.604779	0.732561	0.732561	0.604779	0.729628	0.730606	0.601519	0.732561	0.729302	0.601845
6	0.73028	0.734517	0.604127	0.732561	0.732236	0.604453	0.731584	0.729954	0.601845	0.732236	0.729628	0.601519
7	0.731258	0.730932	0.604453	0.732236	0.73191	0.605105	0.731258	0.731258	0.601845	0.73191	0.734517	0.600867
8	0.73191	0.732561	0.605431	0.73191	0.72539	0.604127	0.731258	0.730932	0.601519	0.73028	0.727672	0.602171
9	0.732887	0.73191	0.603801	0.730606	0.73191	0.604127	0.728976	0.731584	0.58685	0.732236	0.73028	0.601519
10	0.731584	0.73028	0.604453	0.732561	0.732561	0.605105	0.730932	0.730606	0.602497	0.73028	0.729628	0.602497

Figure 6: Positive COUNTY Excel Results

	Pin1 (volts)	Pin2 (volts)	Pin3 (volts)	Pin4 (volts)	Pin5 (volts)	Pin6 (volts)	Pin9 (volts)	Pin10 (volts)	Pin11 (volts)	Pin12 (volts)	Pin13 (volts)	Pin14 (volts)
2	-0.693255	-0.693907	-0.460509	-0.692278	-0.693581	-0.479416	-0.694885	-0.693255	-0.315776	-0.693907	-0.694233	-0.453663
3	-0.693581	-0.692278	-0.310234	-0.674675	-0.621867	-0.201358	-0.695537	-0.698145	-0.355545	-0.694233	-0.694233	-0.424652
4	-0.693255	-0.694559	-0.429541	-0.694885	-0.696189	-0.435083	-0.694885	-0.693581	-0.236564	-0.693907	-0.695863	-0.370214
5	-0.693255	-0.694233	-0.061841	-0.69293	-0.69293	-0.455945	-0.697167	-0.698145	-0.454641	-0.694559	-0.695537	-0.351959
6	-0.692278	-0.694233	-0.474852	-0.691952	-0.691952	-0.356849	-0.695537	-0.694559	-0.457575	-0.694559	-0.69293	-0.375755
7	-0.691626	-0.691626	-0.311212	-0.693581	-0.695537	-0.275029	-0.689344	-0.696515	-0.353589	-0.694559	-0.695537	-0.452686
8	-0.693255	-0.693581	-0.475178	-0.694233	-0.692278	-0.448774	-0.697819	-0.694233	-0.482675	-0.694233	-0.6913	-0.423674
9	-0.691952	-0.69293	-0.339572	-0.695537	-0.693907	-0.407375	-0.696515	-0.696841	-0.462465	-0.615673	-0.695863	-0.439972
10	-0.694233	-0.693581	-0.407049	-0.695211	-0.693255	-0.413894	-0.696841	-0.694885	-0.344136	-0.694233	-0.695863	-0.445514
11	-0.690974	-0.693255	-0.301433	-0.693907	-0.693581	-0.453012	-0.697167	-0.695863	-0.357175	-0.694559	-0.695211	-0.354567

Figure 7: Negative COUNTY Excel Results

POSTIVE AVERAGE		
Input Pins		Output Pins
0.728373		0.590843

NEGATIVE AVERAGE		
Input Pins		Output Pins
-0.65819		-0.39706

Figure 8: Negative and Positive COUNTY Average Results

The outputs are highlighted in yellow in Figures 6 and 7. For the positive tests, all the output results are .59 to .6 V drops across the diode. For negative tests, the results were between -.3 to -.4 V drops. This information could mean that different diodes are used on the outputs. Typically, over or under voltages are not applied to the output pins of the device during normal operation.
Thus, cheaper ESD diodes are probably implemented instead of the quality ESD diodes on the input pins.

VOH and VOL
These tests are performed the test the minimum voltage that is an output logic HIGH (VOH) and the maximum voltage that is an output logic LOW (VOL). The expected outputs are given by the datasheet and are used to determine the USL and LSL used for statistical analysis. Current is sourced during VOH tests as the device is forced to mimic the DUT driving a load, and current is sunk into the device during VOL to simulate some *other* device downstream driving the DUT.

For VOH, 5 mA is sourced from each pin-under-test. This is done by connecting a suitable resistor to GND. After some calculations, 1 kΩ was chosen. .99 kΩ was the real value after measuring with an ohmmeter. The digital multimeter on the MyDaq was used to confirm the expected current when tests were performed, as shown in the figure on the following page. The result is shown in Figure 9 and 10.

Output Voltage	Current w/Resistor
5.2	5.25E-03
5.3	5.35E-03
5.4	5.45E-03
5.5	5.56E-03
5.6	5.66E-03
5.7	5.76E-03



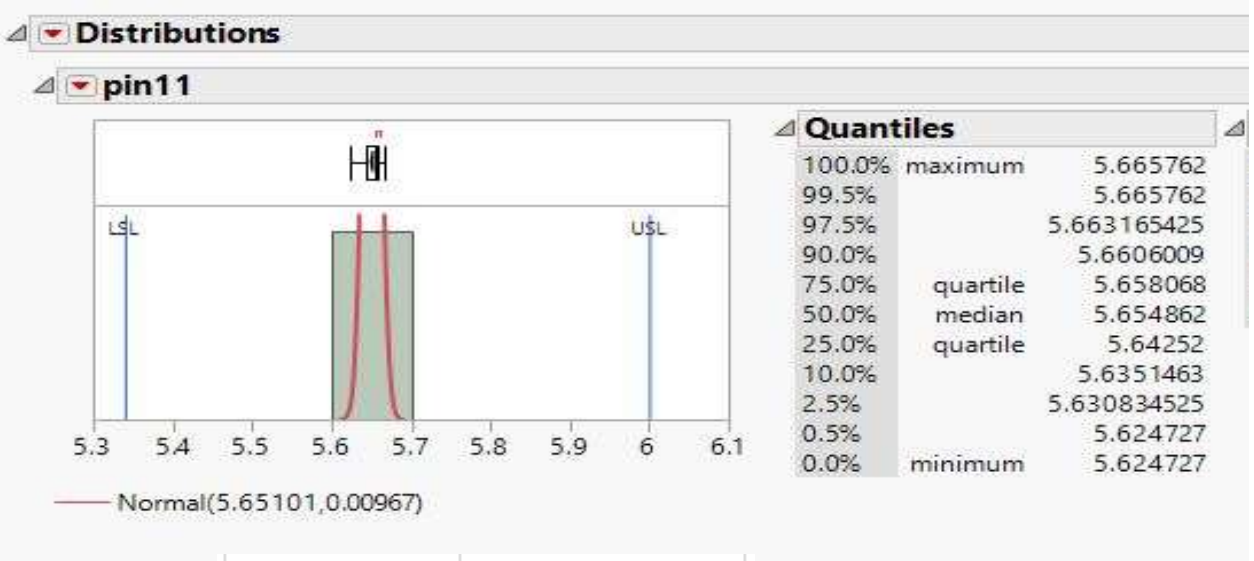
Figure 9: VOH Current Values



Output Voltage	Current w/Resistor
0.15	5.91E-03
0.16	5.90E-03
0.17	5.89E-03
0.18	5.88E-03
0.19	5.87E-03
0.2	5.86E-03

Figure 10: VOL Current Values

As shown above, 5 mA is sourced/sunk even during the output voltages that are off target for both VOL and VOH. According to the datasheet, 5.34 to VCC is anticipated for a logic high, and .33 to GND is expected for a logic low. A sample of statistical analysis is presented below.



Output Voltage	Current w/Resistor
0.15	5.91E-03
0.16	5.90E-03
0.17	5.89E-03
0.18	5.88E-03
0.19	5.87E-03
0.2	5.86E-03

(only **magnitude** of current is given)

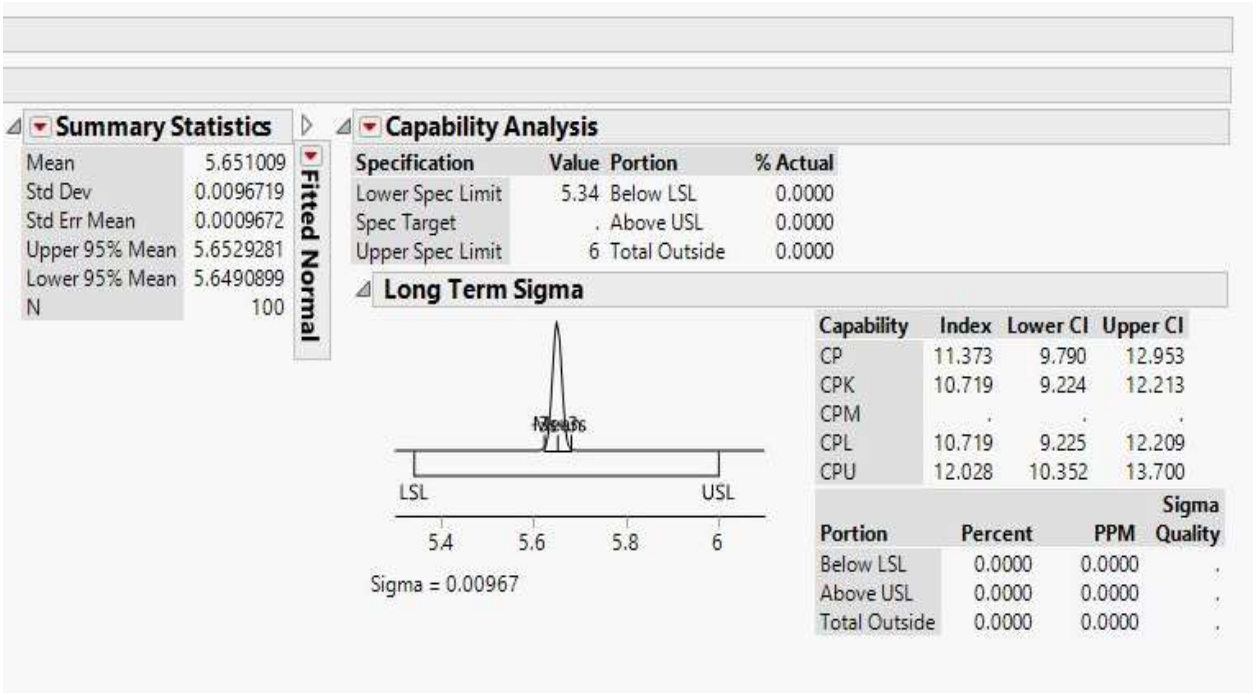
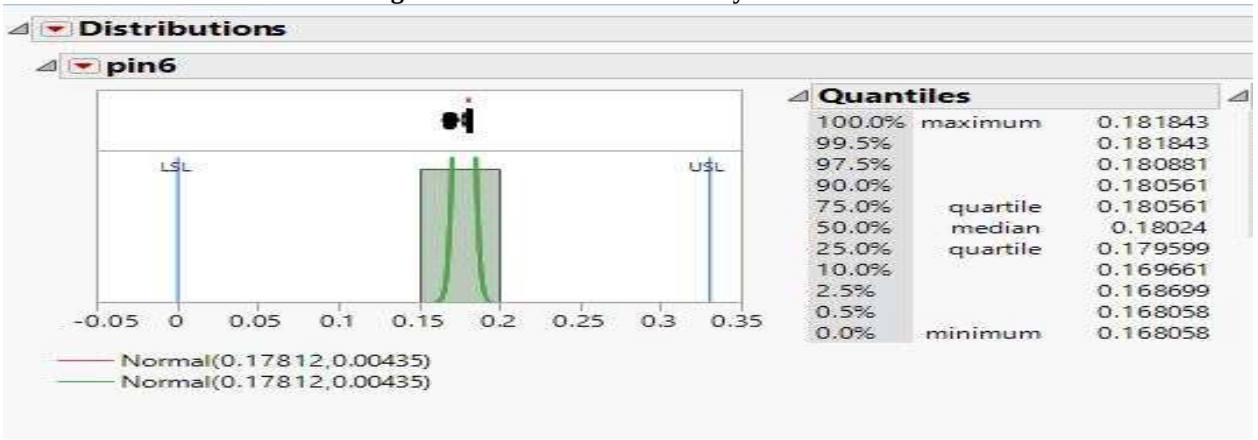


Figure 11: VOH Statistical Analysis



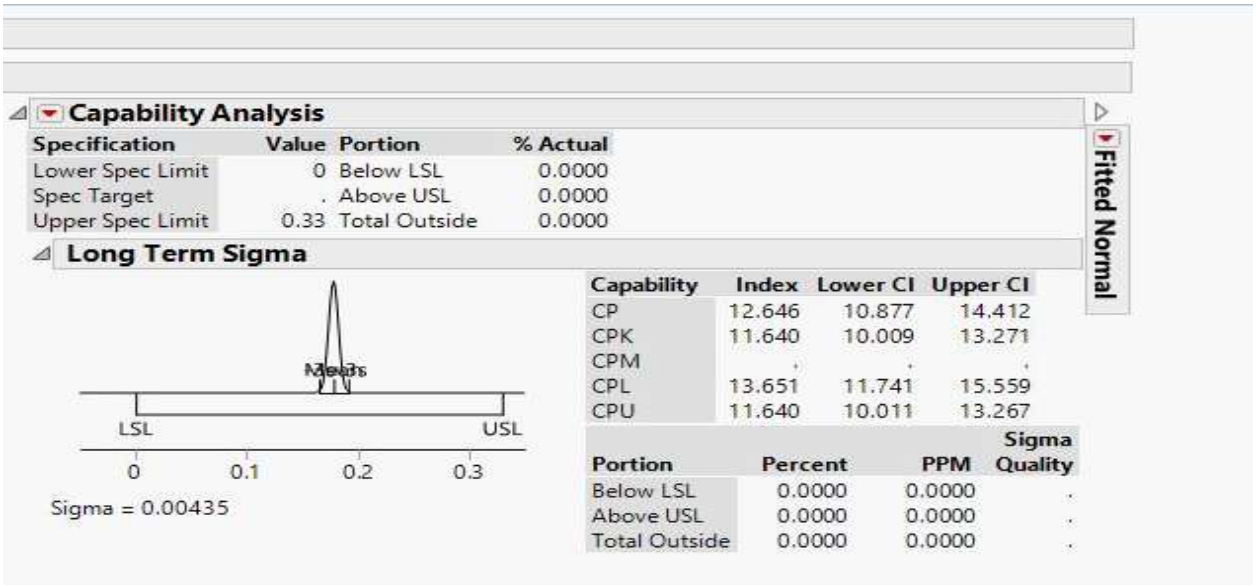


Figure 12: VOL Statistical Analysis

The CP and CPK values were around 10 to 15. These are good numbers as they are above 2 and 1.5 respectively. This means that our instruments measured consistently, with low noise, and that the actual output of the DUT was also consistent AND accurate. This can be explained by the constant DC voltages applied to the input pins, as opposed to AC signals or quickly.

The CP and CPK values were around 10 to 15. These are good number as they are above 2 and 1.5 respectively. This means that our instruments measured consistently, with low noise, and that the actual output of the DUT was also consistent AND accurate. This can be explained by the constant DC voltages applied to the input pins, as opposed to AC signals or quickly oscillating signals that would definitely introduce noise into the system (as in the case of VIH and VIL).

VOH and VOL Code

The code is as follows: of the two input pins of a single NAND gate, both are held at some VIH or VIL voltage. For VOH, both inputs are held at VIL. For VIL, both are held at VIH- as specified by the datasheet. While both inputs are some voltage, the output voltage is measured and written to an excel datasheet. This is done 100 times in a for-loop and then a normal distribution is generated.

The LabView code structure for VOL is very similar to that of COUNTY. The limits are changed to 0 and .33. For VOH, the limits are 5.34 and 5.99. A logic high for the comparator is a pass. Additionally, the actual measurement garnered by the DAQ Assistant is recorded in an Excel file.

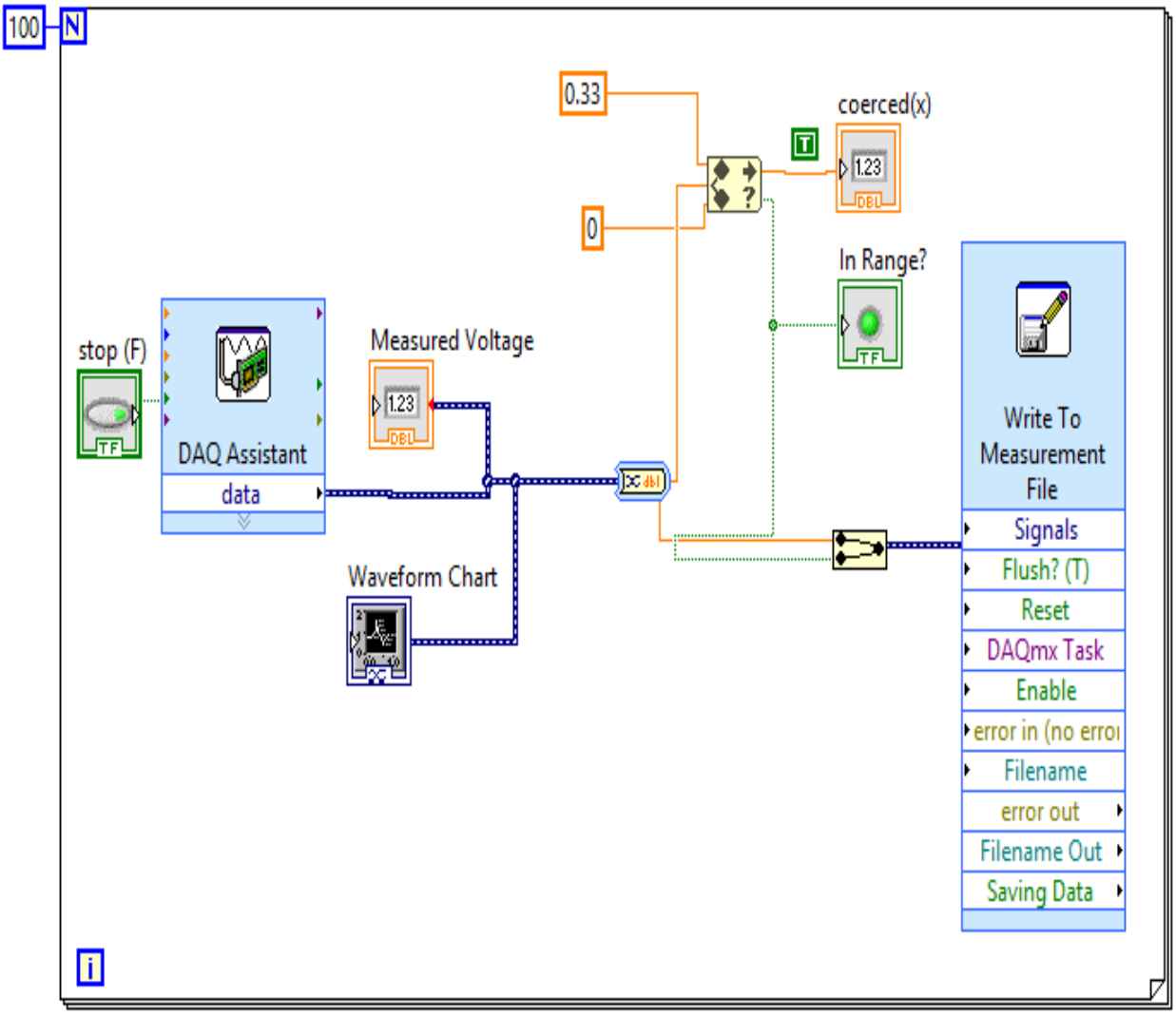


Figure 13: VOL Code

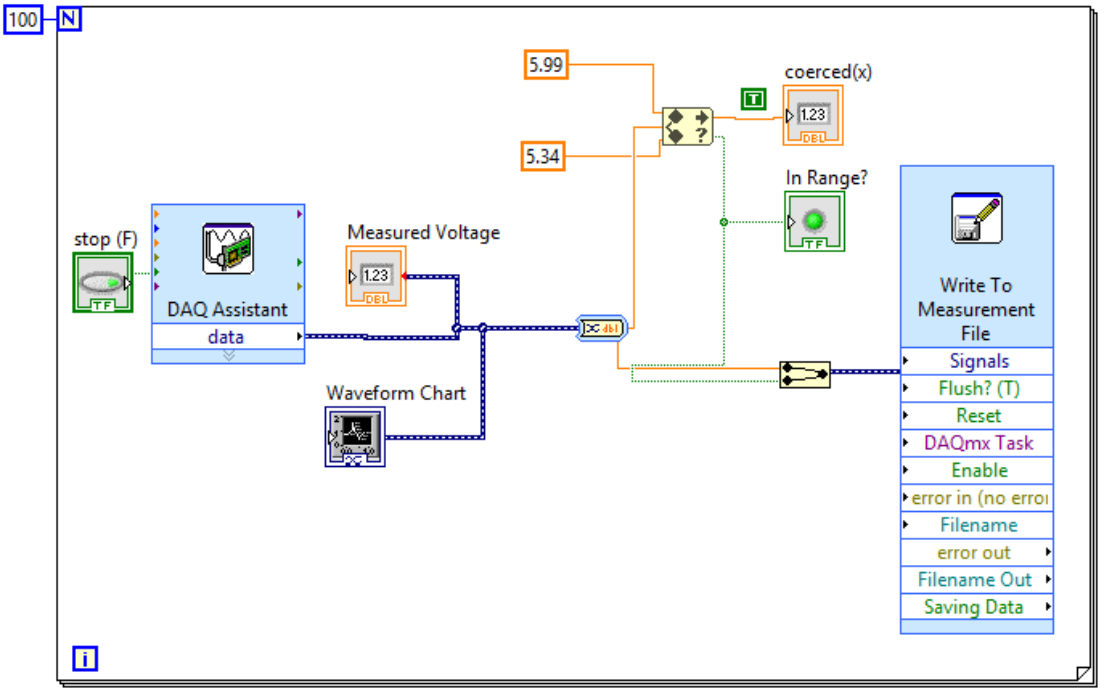


Figure 14: VOH Code

	Pin3 (volts)	Pin6 (volts)	Pin11 (volts)	Pin14 (volts)
2	0.173187	0.171884	0.169276	0.167646
3	0.172536	0.170906	0.171884	0.166994
4	0.172862	0.17221	0.171232	0.168624
5	0.17221	0.17058	0.171232	0.166016
6	0.172862	0.170906	0.171558	0.16895
7	0.17221	0.170906	0.169928	0.167972
8	0.171884	0.171884	0.171232	0.16895
9	0.172536	0.170254	0.170254	0.16732
10	0.173187	0.17058	0.171884	0.168624
11	0.173513	0.171232	0.172536	0.168298
12	0.172862	0.170906	0.170906	0.16732
13	0.172536	0.171232	0.171884	0.168624
14	0.173187	0.171232	0.17058	0.169276
15	0.166668	0.170906	0.17058	0.167972
16	0.173187	0.171232	0.169276	0.167646
17	0.172536	0.171558	0.17058	0.168624
18	0.17058	0.17058	0.17058	0.166342
19	0.171884	0.171884	0.170906	0.166994
20	0.172862	0.170906	0.173187	0.167646
21	0.173839	0.170254	0.171232	0.167972
22	0.172536	0.171232	0.171884	0.167972
23	0.16406	0.17058	0.170254	0.16732
24	0.170906	0.169928	0.171558	0.168624
25	0.166016	0.170254	0.171232	0.168298

Figure 15: VOL Excel Data

	A	B	C	D
1	Pin3 (volts)	pin6 (volts)	pin11 (volts)	pin14 (volts)
2	5.753889	5.766276	5.774751	5.776055
3	5.754215	5.76758	5.776055	5.774751
4	5.754541	5.76758	5.775077	5.774751
5	5.753563	5.767906	5.776707	5.776381
6	5.753563	5.769535	5.776055	5.776707
7	5.754215	5.768557	5.774751	5.775403
8	5.753237	5.768883	5.773773	5.775403
9	5.754541	5.769861	5.774425	5.776707
10	5.753563	5.770839	5.774425	5.775729
11	5.755518	5.771817	5.775729	5.776055
12	5.755192	5.770187	5.776055	5.776055
13	5.755518	5.770839	5.776707	5.774425
14	5.755192	5.769861	5.775729	5.777685
15	5.75617	5.770839	5.776055	5.776055
16	5.755518	5.767906	5.776707	5.776055
17	5.756496	5.768232	5.776055	5.775403
18	5.756496	5.770187	5.775403	5.776055
19	5.755192	5.767906	5.776707	5.776707
20	5.756822	5.769209	5.777685	5.775403
21	5.757148	5.768557	5.778337	5.776055
22	5.755844	5.768883	5.777033	5.775077
23	5.755844	5.76758	5.776055	5.775403
24	5.755844	5.76758	5.777033	5.776055

Figure 16: VOH Excel Data

According to the above Excel data, the results of the tests were satisfyingly similar to the numbers projected by the datasheet. The 400 values of each test (100 test per the 4 output pins) were averaged together using the SUM function of Excel.The figure 16 of these averages is presented on the following page.

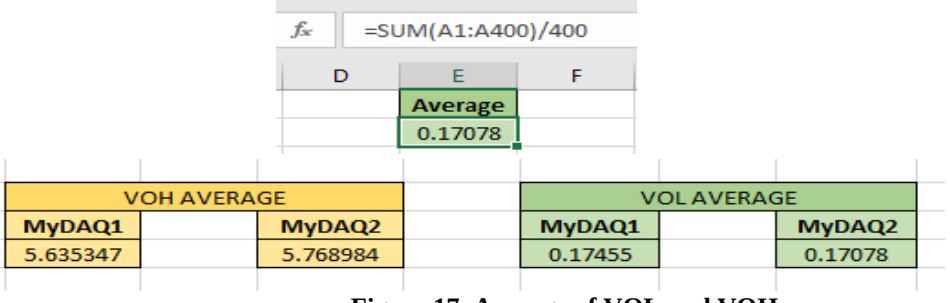


Figure 17. Average of VOL and VOH

Conclusion

In conclusion, the testing provided some very illuminating results. The presence of the output diodes was unexpected, as was the notably low CP and CPK values for the VIL and VIH tests. This is accounted for by the sweep changing quickly with close to no settling time. This is one limitation of the instrument that was not planned for. Additionally, the GR&R was higher than predicted. This can perhaps be explained by user error and environmental variables.

The NAND gate was chosen for testing because of its simplicity and consistency. With primarily digital tests, the focus could be attached to understanding the needed LabView code to read inputs and outputs, store data, provide sweeps, etc. The simplicity of the device's circuitry and resulting tests also allowed for more time to experiment with different instruments like multiple MyDaqs and the Virtual-Bench. The bench was a pleasure to use as it was a reliable power supply, could easily sink and source the needed currents, and provided an oscilloscope function for confirmation of results.

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