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Design and simulation of Class A amplifier with 10W power S-band applied in radar systems using PHEMT transistor

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Abstract

Amplification the received signals is very important and integral in communication systems (transmitter, receiver, radar and etc…). Amplifiers, as separate blocks, get the signal to the desired level in several stages, depending on the amount of amplification required. The power amplifiers are the most widely used in transmitters of radio frequency (RF). The output power level is more important that other parameters at the power amplifier design. In this paper, the ADS software is used to design and achieve the optimum parameters of a power amplifier in a frequency band S with the output power level 40dBm, gain 21dB and the noise less than 6dB. The better results have been obtained using optimization techniques that are in a large extent comparable and competitive with the products of foreign companies.

Keywords: Band S, transmitter of radio frequency, power amplifier, PHEMT

Introduction:

There is conventionally and commonly an increasing demand for transmitter-receiver modules (T/R) of S-band radar for military, general and space use. In T/R systems, high power amplifier module has the maximum current consumption and the largest T/R system in radar. To obtain a high power in module or plan, we should be developed preferably as a MMIC to minimize and reproducibility of module (D Hecht et al., 2005) (Bush et al., 2005). Thus, the method for power combination for high power output and small size chip is very important. The linearity of radio frequency power amplifier plays an important role for expressed applications. This paper simulates the design and simulation of band S MMIC power amplifier, 10-watt, with a two-story circuit.

The Stages of Amplifier Design

Overall stages of design can be considered as the selection of transistor, the selection of a suitable operating point, checking the stability of the transistor, application of the feedback circuits and finally the matching circuit design which each of the cases will be mentioned below.

The schematic of this amplifier is shown in Figure 1.

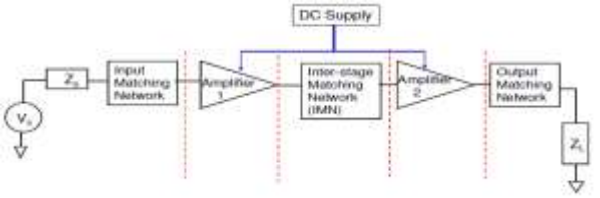


Figure 1: General Topology of Amplifier

The Selection of Transistor

The first step in designing an amplifier is the suitable selection of a transistor as required. With regard to the issue, selective transistor should have the desired function in the desired frequency range and also production capability and output power tolerance. Usually cut-off frequency of the transistor must be at least 10 times larger than the central frequency. The transistor pHEMT-fED2ONl1 has been selected from design kit transistors. One of the most important characteristics of the transistor that is considered to design and achieve the desired characteristics is the number and width of finger. The direct effect of the two parameters is on the amount of the tolerable power and drain current of the transistor that is crucial in an optimum operating point. Of course, the breakdown voltage of the transistor should be changed to match the optimum operating point, and it is usually considered 3 times larger than the bias voltage.

The Selection of Optimum Operating Point

The load line technique is used to choose a suitable bias point of transistor (D Hecht et al., 2005). The output power is 40dBm and load resistance normally is 50Ω. With regard to this chart and the selection of a reasonable amount for V_{DD}, we can achieve an approximation amount from transistor I_{peak}. To have a safety margin, the flow rate is selected slightly higher than this value. For high linear range, the current of bias point of the transistor is selected half of the maximum drain current. Reaching the maximum flow rate depends on the suitable selection of the number and width of the transistor fingers. According to the calculations, the optimal bias point of transistors is selected as follows.

V_{GS2}=-0.95v, V_{GS1}=-0.8v
$V_{DS1,2}$=15v
ID1=190mA, ID2=2.3A

The Stability of Transistor

After stabilizing the bias voltages, the transistor stability situation must be assessed in terms of bandwidth. With the simulation in ADS (Figure 2), this transistor is unstable in a part of the band and the transistor should be stable band before anything is done.

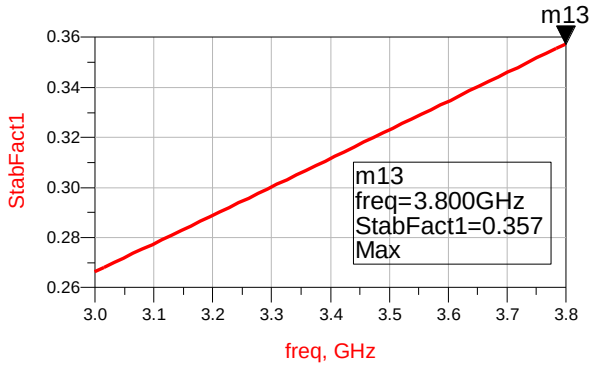


Figure (2): The coefficient of transistor stability before feedback application

The Feedback Circuits

The use of feedback circuits is one of usual methods for stability of transistor. After applying the feedback circuit to the transistor, the parameter K which shows stability of the transistor, is shown in Figure 3 which is in the frequency range K> 1 and as we can see, the minimum value equal to 71 and the transistor stability is guaranteed.

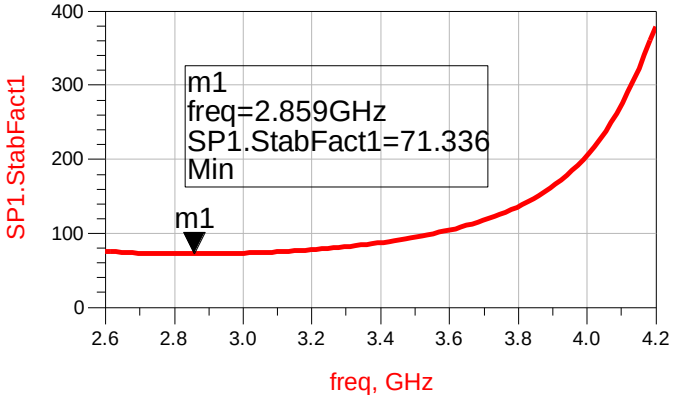


Figure (3): The graph of transistor stability by applying the feedback circuit

Designing the matching circuit

The matching circuits in output are used to have a higher output of power amplifier. The first stage and second stage amplifier designed circuit are shown in tables 3 and 4. The design is achieved by fitting the proper matching topology and using both compressed and distributed elements (Florian et al., 2005). In the design of power amplifier, the output matching network which passes the maximum output power from FET to 50 ohm load should also be designed. The Load Pull simulation should be effectively done using the software to determine power and load contours and then the optimized large signal load impedance Z_{opt} is achieved. The tuning simulation is done to design better the circuit.

.2

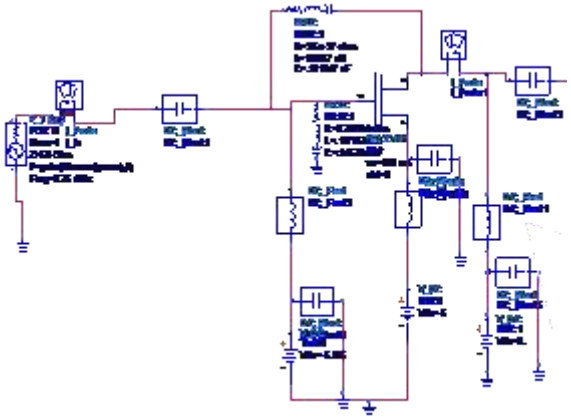


Figure 3: The first stage general designed circuit without the matching circuits

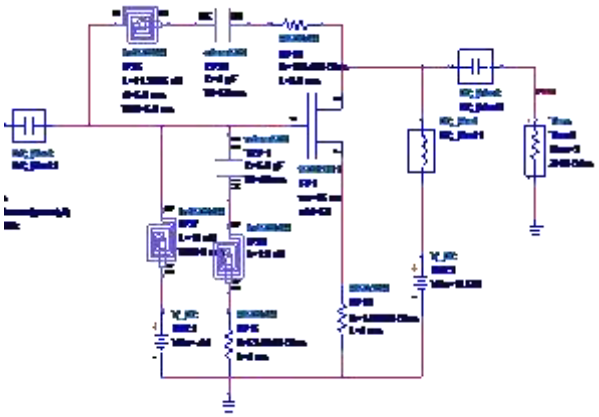


Figure 4: The first stage designed general circuit without the matching circuits

The Design Results

In Figure 5, the dispersion parameters S_{11}, S_{12}, S_{22} are shown and as we can see the circuit gain about 21dB with the appropriate matching in input and output is obtained.

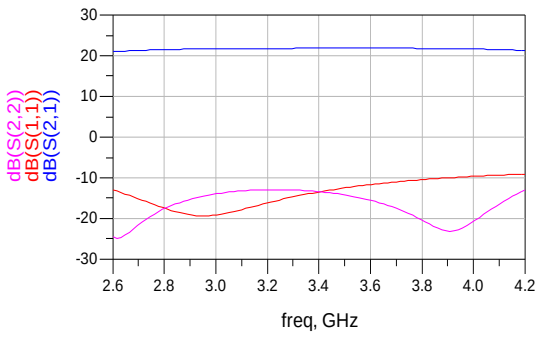


Figure 5: Input internal losses (S_{11}) and output internal losses (S_{22}) and large signal gain (S_{21}) in terms of frequency

It should also be noted that ripple S_{21} is 0.8 dB, which seems very appropriate. Drain voltage and current are15v, 2.3A, respectively. In Figure 6 you can see that the noise figure is in the range of 6dB by applying Tuning that is acceptable to the amplifier.

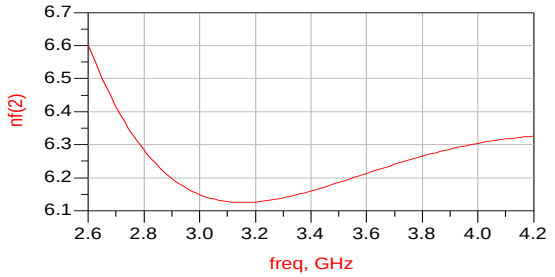


Figure 6: The graph of Noise figure (nf) in terms of frequency

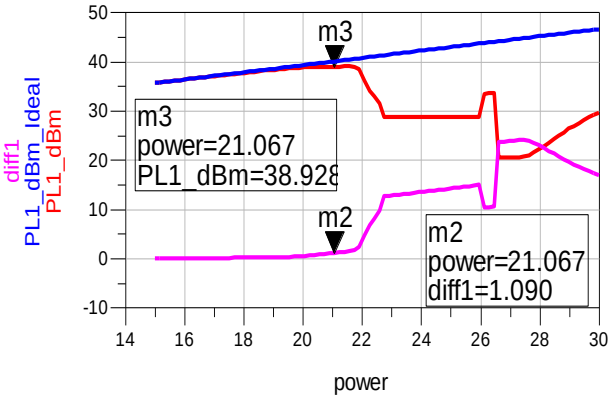


Figure 7: The output power in terms of input power from the amplifier in Vd = 15v

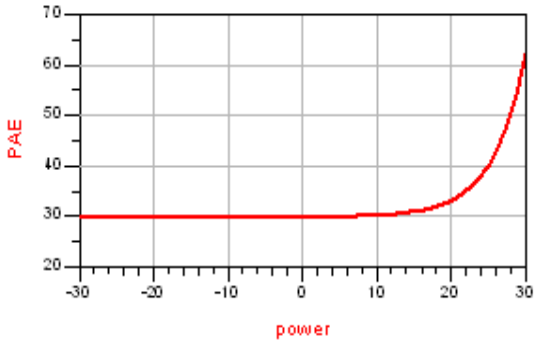


Figure 8: The power-added efficiency (PAE) from the amplifier in terms of input power in Vd = 15v

Figures 8 and 9 show the output power in terms of input power and PAE related to the amplifier on the input power at the central frequency of 3.4 GHz, respectively. The amplifier presents a maximum output power equal to 40dBm with 32% of PAE at the central frequency of 3.4 GHz and 20.5dB of S_{21}. On the bandwidth of 2GHz, the output power higher than 40dBm with a very flat PAE between 30% and 33% can be concluded.

3. Conclusion

A high power amplifier in a two-stage is designed for radar applications in S-band. The design has been done using transistors with a gate length of 0.5um and GaAs pHEMT technology. The output power of the circuit is 40dBm with %32 and gain 20.5dB in S frequency band S.

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