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Novel Efficient Designs for QCA JK Flip flop Without Wire-crossing

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Abstract

Recently, the conventional CMOS technology faces serious challenging problems due to the physical limitations in its feature size reduction. Quantum dot cellular automata (QCA) with having the higher speed, smaller size and lower power consumption has the potential to be one of the features promising nanotechnologies to replace CMOS technology. In this paper, novel efficient designs for QCA JK flip flop without wire-crossing are presented. The proposed JK flip flops are designed and tested in QCADesigner software. In comparison with the previous QCA and CMOS JK flip flops, our designs are optimized in terms of cell count, area, power and delay. Therefore, these structures can be used in designing of QCA based circuits.

Keywords: Quantum-dot Cellular Automata, CMOS Technology, QCA Cell, QCADesigner, JK Flip flop

Introduction:

Quantum-dot Cellular Automata (QCA) (Wilson, 2002; Askari, 2008) relies on new physical phenomena, and innovative techniques that radically depart from a CMOS-based model. The QCA cell (Sheikhfaal, 2015; Teja, 2008) is the fundamental unit of QCA, which created with 4 quantum dots and 2 electrons as shown in Figure 1(a). In QCA technology, the binary information is encoded in the 2 possible polarizations (P= +1 to represent logic ”1” and P=-1 to represent logic ”0”). QCA devices can be constructed using different cell arrangements (Lent, 1993; Sayedsalehi, 2011). The binary wire and inverter chain are 2 types of QCA wire as shown in Figure 1(b). The binary signal propagates from input to output in a QCA wire because of the electrostatic interactions between the cells. The QCA inverter gate

is shown in Figure 1(c), which is usually formed by placing the cells with only their corners touching. Figure 1(d) shows the QCA majority gate, which performs a function given by the following equation:

$$f = M(a,b,c) = a.b + a.c + b.c \quad (1)$$

The schematics of the inverter and majority gates are shown in Figure 1 (e) and Figure 1(f), respectively. Using the QCA wires, inverters and majority gates, any QCA circuit can be implemented.

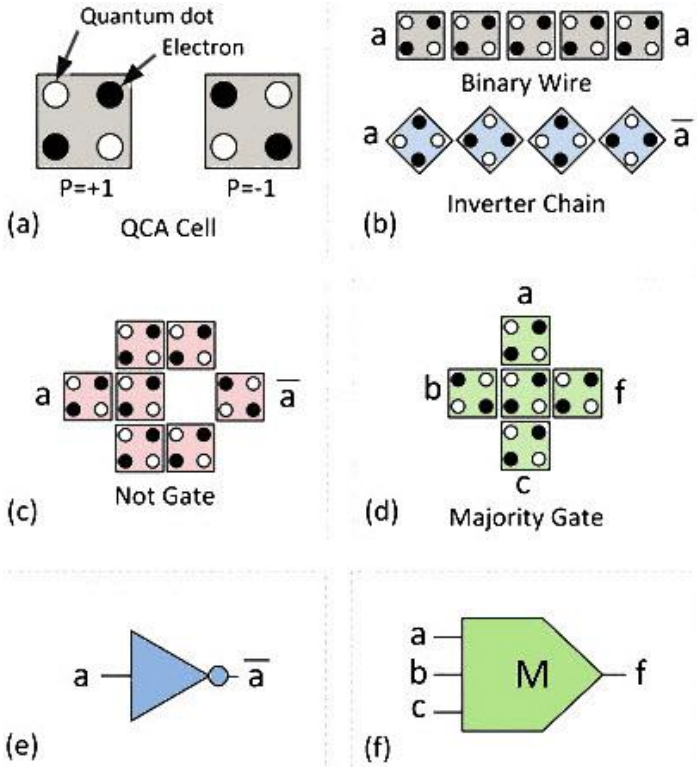


Figure 1. QCA basis components.

In (Rahi, 2015), conventional CMOS techniques used for JK flip flop have been compared and their surface area and consumed power has been computed. In (Vetteth, 2003) few layouts for all the flip-flops have been proposed, which work with ultra-low power consumption and very high operating speeds. In (Kaphungkui, 2014), optimized implementations of the flip-flops have been presented which are level triggered and negative edge triggered using CMOS 180nm Technology. In (Kumar, 2013) the sequential circuit's using different sequential circuit components have been designed. Also, the different characteristics such as power conception and area occupation etc. by sequential circuit have been analyzed using Microwind software. The design of low power, high performance JK flip flop has been presented in (Pinki, 2015). In this paper, novel efficient designs for QCA JK flip flop without wire-crossing are presented, which are optimized in terms of cell count, area, power and delay.

Design approach:

A JK flip flop is a refinement of the SR flip flop, in which the indeterminate state of the SR type is defined in the JK type. In a JK flip flop, the input J is for set and the input K is for clear. The inputs J and K in a JK flip flop behave like the inputs S and R in a SR flip flop to set and clear the flip flop. When both J and K inputs are set to logic 1, the flip flop switches to its complement state, i.e., if Q=1, it switches to Q=0 and vice versa (Q is the output). The Output Q is ANDed with K and Clock inputs so that the flip flop is cleared during a clock pulse only if Q was previously 1. Similarly, output $\overline{Q_o}$ is ANDed with the inputs J and Clock so that the flip flop is set with a clock pulse only if $\overline{Q_o}$ was previously 1. Because of the feedback connection in the JK flip flop, the Clock signal, which remains at 1 after the outputs have been complemented once, will cause repeated and continuous transitions of the outputs. To avoid this undesirable operation, the Clock pulse must have time duration, which is shorter than the propagation delay through the flip flop. Since the circuits implemented with QCA are the clock base circuits, there is no need to show the input Clock in the equivalent QCA JK flip flop. Therefore, if the input set in QCA JK flip flop is {JK}={00, 01, 10, 11} then the output will be {Q}={Q_o, 1, 0, $\overline{Q_o}$ }, where Q_o is the previous value of the output Q. This relationship between the inputs and output of the QCA JK flip flop is equivalent to one of the following equations:

$$Q = K.\overline{Q_o} + \overline{J}.Q_o \tag{4}$$

$$Q = M(K.\overline{Q_o}, \overline{J.Q_o}, Q_o) \tag{5}$$

$$Q = (K + Q_o).(\overline{J.Q_o}) \tag{6}$$

Figures 2a-2c show the equivalent circuit diagram for QCA JK flip flops implemented by the inverters and majority gates for Equations (4)-(6), respectively. The flip flop shown in Figure 2a is constructed using 3 majority gates and 2 inverters. The circuit has two inputs J and K. The output Q of the flip flop is fed back to the majority gate (with the input J) and the complement of the output is fed back to the input majority gate (with the input $\overline{J}$). The outputs of these majority gates are Anded to produce the output Q.

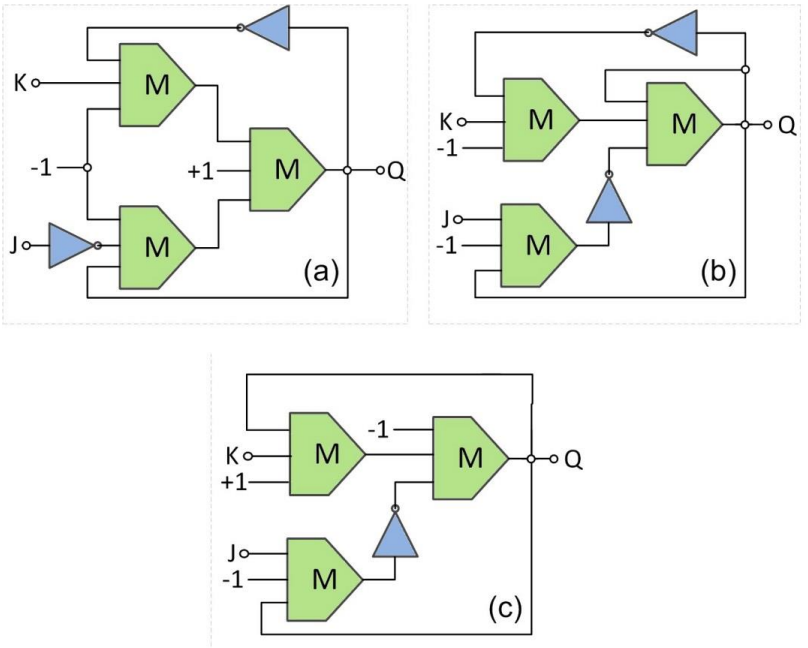


Figure 2. Circuit diagram of the proposed JK flip flops.

Because of their different clocking schemes, the design of QCA sequential circuits is quite different from the design of traditional CMOS sequential circuits. In this paper, we proposed the optimized QCA JK flip flops, which require minimum area, number of cells and clock phases. The equivalent QCA implementations of the proposed JK flip flops shown in Figure 2a-2c are shown in Figure 3a-3c, respectively. These layouts are achieved using cell minimization techniques. As shown in Figure 3, the proposed layouts are designed in one layer without wire-crossing. The input to output delays for all gates and functions in Figure 3a-3b are 4, 6 and 5 clock phases, respectively. As shown in Figure 3, the most optimized design is the QCA JK flip flop shown in Figure 3a. Therefore, we can use this structure to compare with the previous designs. The specifications of the proposed QCA JK flip flop shown in Figure 3a are as follow: number of QCA cells 20, approximated area 0.016 μm^2, approximated wasted area in cells 20 and delay (number of clock phases) 4. Also, its consumption power is 10^{-10}W, because the consumption power in the QCA arrays is 10^{-10}W per input bit (Lent, 1993). The delay for this flip flop is 1 clock cycle. Therefore, each circuit has four clocking zones. Initially clock 0 is used to get the inputs. Clock 1 is used to route inputs for majority gate logic and find majority logic and clock 2 is used to compute the output. Finally, the output is available at clock 3.

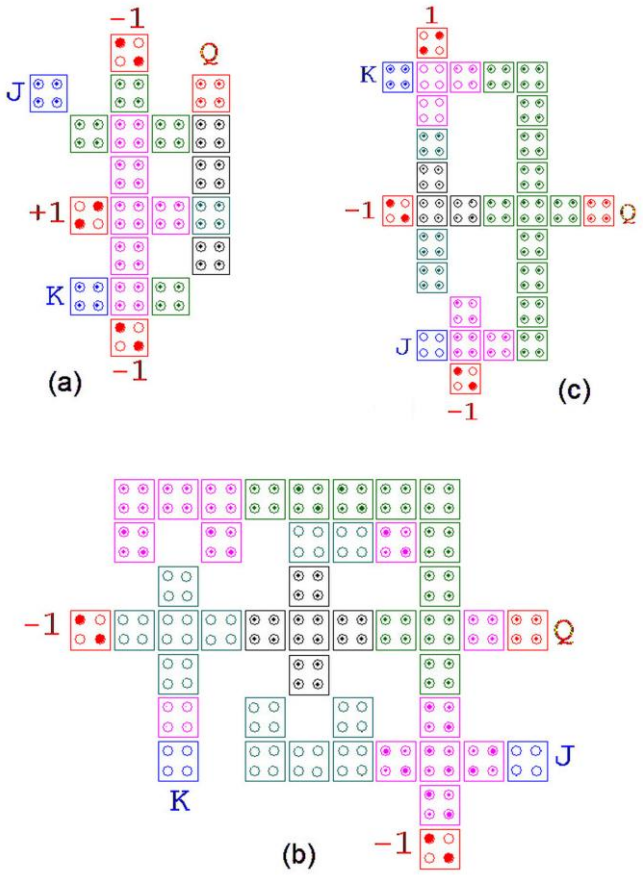


Figure 3. QCA implementation of the proposed JK flip flops.

Results and discussion:

Figure 4 shows the input and output waveforms for the proposed JK flip flop designs. This simulation results are obtained using QCADesigner software version 2.0.3 (Mina, 2016), which verify the functionality of the proposed flip flops. The following parameters are used for a coherence vector engine: temperature 1 K, relaxation time 1 fs, time step 0.01 fs, total simulation time 7 ps, clock high 9.8×10^{-22} J, clock low 3.8×10^{-23} J, clock shift 0, clock amplitude factor 2, radius of effect 65 nm, relative permittivity 12.9, layer separation 11.5 nm, Euler method, and randomized simulation order. Also cells are assumed to have a width and height of 18 nm, the neighbor cells have a center to center distance of 20 nm and quantum dots have 5 nm diameters. Table 1 shows the comparison between our designs with the CMOS technology and previous QCA designs. As it is seen from Table 1, in comparison with the best previous QCA design presented in (Kungkui, 2015), the important improvements (percentage reduction) achieved for the best proposed QCA JK flip flop shown in Figure 3a are 55% in the area, 56% in cells count and 72% in the wasted area in the cells, where the important improvement (II) is obtained by the following equation:

$$II = (1 - \frac{X}{Y}) \times 100 \quad (7)$$

where X and Y stand for the measured objects (area or cell count, …) for our design and the previous designs, respectively. Whereas their power consumption and input to output delay are same. In comparison with Reference (Vetteth, 2013), the important improvements are 83% in the area, 77% in cells count and 87% in the wasted area in the cells. Also, our design has less power consumption than the previous design presented in (Vetteth, 2013). From these results, it is clear that the proposed design is better than the previous QCA works. Also, in Table 1 we have compared our QCA designs with the conventional CMOS technology. Our best design has 850 and 631 times less power consumption and area, respectively than the JK flip flop implemented with 45 nm CMOS Technology presented in (Rahi, 2015). In comparison with the JK flip flop implemented with 0.18 um CMOS Technology presented in (Kaphungkui, 2014), our best design is more than 70000 times faster. Also, it has a power consumption approximately 32000 times less than the CMOS JK flip flop presented in (Kaphungkui, 2014). From these results, it is clear that the QCA designs are more efficient in terms of area, power and delay in comparison with CMOS technology. The obtained results show that the proposed QCA JK flip flops work satisfactorily and produce the required results. The implementation of this design may lead to the efficient use of complex circuits in the various applications, which may be a future technical advancement of this work.

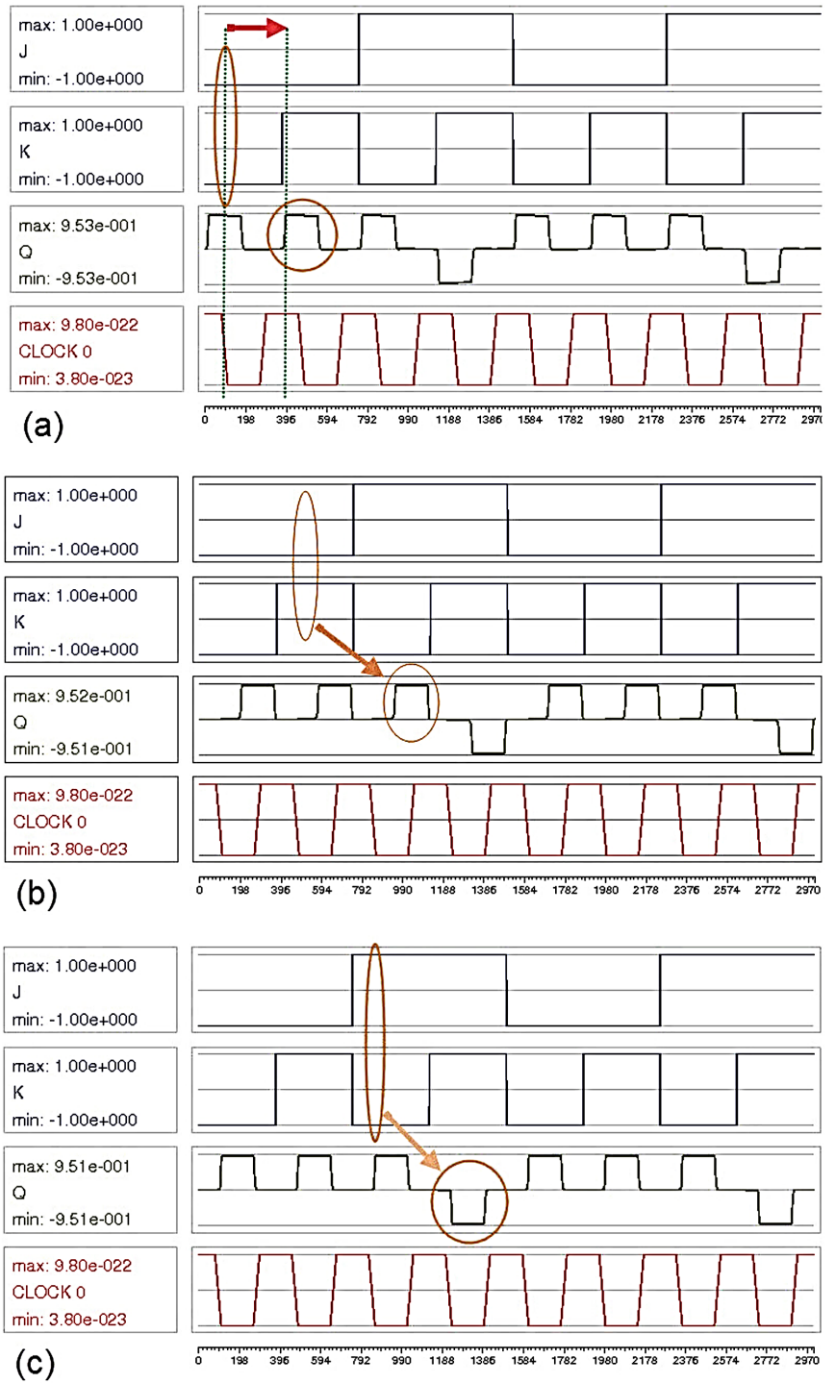


Figure 4. Simulation results of the proposed QCA JK flip flops.

Table 1. Comparison with CMOS technology and previous QCA designs.

References	Power (μW)	Approximated area (μm^2)	Propagation delay (ps)	Approximated wasted area in cells	Cell count	Delay (clock phase)
45 nm CMOS Tech. (Rahi, 2015)	0.17	10.1	-----	-----	-----	-----
65 nm CMOS Tech. (Rahi, 2015)	0.89	19.7	-----	-----	-----	-----
90 nm CMOS Tech. (Rahi, 2015)	5.33	40.3	-----	-----	-----	-----
0.25um CMOS Tech. (Kumar, 2013)	82	572.2	-----	-----	-----	-----
0.18um CMOS Tech. (Kaphungkui, 2014)	6.51	-----	20000	-----	-----	-----
45nm CMOS Tech. (Pinki, 2015)	0.387	10.5	-----	-----	-----	-----
QCA JKFF (Kungkui, 2015)	0.0002	0.036	-----	74	46	4
QCA JKFF (Vetteth, 2003)	0.0003	0.098	-----	157	90	4
Proposed JKFF (Figure 3a)	0.0002	0.016	0.281	20	20	4
Proposed JKFF (Figure 3b)	0.0002	0.039	0.468	53	45	6
Proposed JKFF (Figure 3c)	0.0002	0.030	0.375	47	30	5

Conclusion:

In this paper, novel JK flip flops for implementation in QCA is presented. For simulation of the proposed layouts QCADesigner software is used. The proposed designs are compared with the other previous QCA works. The results show that our best design has the minimal size and cell count, and it is implemented with only four clock phases. Also we have compared the proposed QCA JK flip flops designs with the conventional CMOS technology. The results confirm that the QCA designs are more efficient in terms of area, power and clock frequency.

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