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Improving the implementation of ADPLL using LC Voltage Controlled Oscillator

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Abstract

A Digitally Controlled Oscillator (DCO) which is presented in this paper is a main part of an All-Digital PLL because of their critical role in ADPLL foundation. Since some challenges are available such as quantization noise and the limitations in LC oscillators that they cause to dither the frequency control word make the DCO's operation undesirable. But in the proposed method, problems removed due to high performance by the solution of employing a delta-sigma modulator and a Voltage Controlled Oscillator. The proposed idea focused on LC oscillator performance to reach the better structure of ADPLL using CMOS process. In this architecture, a modified delta sigma modulator and a custom voltage controlled LC oscillator topology is used. By using a 4th order of band pass delta-sigma modulator and PMOS LC Voltage Controlled Oscillator with good phase noise characteristic, the effects of noise on quantization decreased and the output signal improved respectively. The LC oscillator and delta-sigma modulator were implemented by using TSMC 0.18µm technology. As it can be seen, the employed oscillator causes to increase the ability of ADPLL's operation. Improvement in output parameters is the key point of this paper. The simulation results confirm the proposed idea.

Keywords: Digitally Controlled Oscillator (DCO), All-Digital PLL (ADPLL), Delta-Sigma Modulator, Voltage Controlled Oscillator (VCO), LC Oscillator, Band Pass Modulator, Complementary Metal Oxide Semiconductor (CMOS)

Introduction:

The design of controlled oscillators plays an important role in the design process of ALL-DIGITAL PLLs used for frequency synthesis. Various approaches concerning oscillator topology and controlling its frequency do exist (Unterassinger, H et al,2010). Digitally controlled oscillators (DCOs) allow efficient implementation of direct frequency modulation with an all-digital phase locked loop (ADPLL) and a digital control (Staszewski, R et al, 2006).

All the blocks used in ADPLLs, are purely digital or having digital input/output signals. The resulted digital-intensive architectures bring benefits of high level integration and improved programmability (Xu, L et al, 2010).

The DCO have a number of advantages over their analog counterparts, they are more flexible and usually more robust. The DCO uses a Voltage Controlled Oscillator (VCO) based on LC tank. The noise at VCO shows high-pass transfer function as it appears at the output of VCO. If the noise is present in the input signal, then output suffers from noise (Hajimiri.A, 2001).

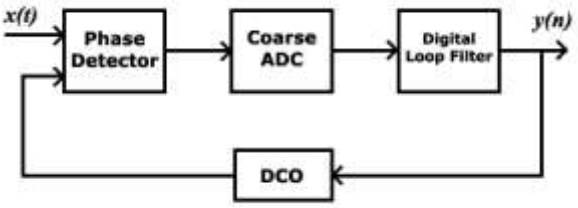
The advanced DCO circuit provides the same tuning range with smaller capacitance loading which is useful for power consumption reduction. In the DCO architecture, one important aspect is designing delta-sigma modulators and the modeling of the quantization noise. An accurate model for this noise is essential for the creation of proper NTFs, which will lead to most effective designs. This shows that when phase and frequency of input signal is unit step, the phase and frequency error of the ADPLL is eliminated by closed loop system.

In this paper, the description of ADPLL features described in All-Digital phase locked loop. The general architecture of the proposed DCO is explained in Digitally Controlled Oscillator (DCO) section. In the following, LC Oscillator Design describes the implementation of voltage controlled oscillator for idea of this paper. The Delta-Sigma Modulator Design includes the study of proposed 4th order band pass delta-sigma structure and then the proposed idea is presented. Finally, the simulated performance of the DCO is provided and discussed.

All-Digital Phase Locked Loop:

The structure of an ADPLL is shown in block diagram form in Figure 1, where the output *y(n)* corresponds to the instantaneous frequency of the input signal *x(t)* (Bourdopoulos, G et al, 2003).

Figure 1: Block diagram of ADPLL



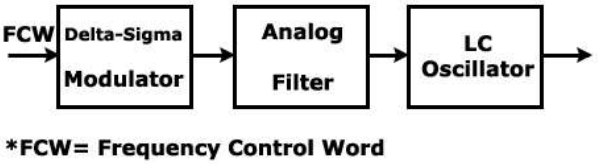
The components of ADPLL are digital Phase detector/comparator, digital loop filter and digitally controlled oscillator where Digital phase detector (kumar, M, 2012) (Kumm. M, 2010) is time to digital converter (TDC). The loop filter is employed in order to obtain the required NTF, which should be high-

pass (for low-pass delta-sigma modulators), as well as the STF, which is desired to be all-pass. This filter is analog and could be implemented either in a continuous time or in a discrete-time active form.
By using fine resolution of Digital Controlled Oscillator (DCO), the phase noise is improved. A digital phase locked loop (Seo, Y. H, 2011) with TDC is implemented using a new concept of floating point number representation which is scaled in resolution according to the amount of input difference.
Various problems in common Digital PLL like noise, leakage, parasitic element etc. can be removed with the help of All-Digital PLL.

Digitally Controlled Oscillator (DCO):

The operation of the DCO is much the same as the operation of dual modulus counter. A DCO circuit is the heart of an ADPLL. The frequency of the DCO is tuned by varactors. A DCO as illustrated in Figure 2, including ΔΣ modulator, an analog filter and an LC oscillator. The LC oscillator which is used in DCO has better phase noise performance than the other structures.

Figure 2: Digitally Controlled Oscillator structure



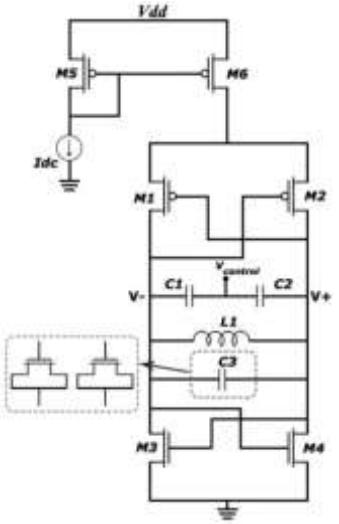
To control the frequency range of oscillator using a digital-intensive approach, digital control words in binary bits are fed into the oscillator. These digital control words are integrated in a DCO core to control the frequency range of oscillator. LC tank plays an important role in oscillation frequency and phase noise performance. The tank inductance and capacitance determine DCO oscillation frequency (Jalil, J et al, 2014).
The DCO performance is based on CMOS scaling, supply voltage, resolution, power consumption and frequency tuning range. Large transistors limit the tuning range of the oscillator caused by increased parasitic capacitance (Staszewski, R et al, 2006).
The effects of decreasing the CMOS scale on the output parameters of DCO are visible in the process of paper idea. Obviously as it can be seen, by decreasing the scales with constant value of the other component, the ability of phase noise and quantization noise suppression increased.

LC Oscillator Design:

Voltage-controlled oscillator is one of the most important modules of the transceivers. The most important parameters which are considered in VCO are low phase noise and power consumption. The VCO phase noise and power consumption in the design will be the opposite of each other, so the design of low phase noise and low power consumption oscillation instruments because of the trade-off between them will be noticeable (Yargholi,M. and Nasri,A., 2015).
An LC-VCO consists of three components: LC tank, tail bias transistor and cross-coupled differential pair. LC tank is made by an inductor and a capacitor connected in cascade or in parallel. Figure 3 shows

the proposed structure of LC-VCO oscillator. Using the VCO topologies has priority to conventional structures due to their above advantages.

Figure 3: Proposed LC-VCO



Increasing the size of differential pair of the oscillator core cause to boost the oscillation frequency. In this paper, the proposed VCO has used PMOS cross-coupled structure to decrease the flicker noise effect. In comparison with NMOS devices, the amount of flicker noise in PMOS devices is lower. In order to calculate phase noise of the oscillator, the best solution is using Leeson's equation as follows:

$$L(\Delta f) \quad g\left[\left(\text{———}\right)\left[F\text{——}\left(1 \quad \text{—}\right)\right]\right] \tag{1}$$

Where f_0 is center frequency, Δf is offset frequency from f_0, Qtank is oscillation tank quality factor, k is Boltzmann constant, and f_c is corner frequency of flicker noise, F is noise factor and T is temperature in kelvin. The frequency tuning range is required to be wide. For wide tuning range the difference between the maximum and minimum values of capacitor would be wide.

Therefore, just using varactors cannot be achieved a wide tuning range. The oscillation frequency of the LC-tank VCO is given as:

$$\omega_0 \quad 1/\sqrt{(C_{var}+C_P+C_{bank})} \tag{2}$$

Where C_{Var} and C_P are the capacitance of the varactors and parasitic capacitor respectively. The oscillation frequency is coarsely adjusted by capacitor bank (C_{bank}) and finely changed by varactors.

When all the capacitors are connected, the frequency range is in the lowest range. While none of the capacitors are connected to tank the highest frequency range is achieved. The digital solution to control the oscillating frequency could be done in the way of weighted binary switchable capacitance devices that

such mentioned above varactors are used. An array of varactors could be switched into a high or low capacitance mode individually by a two-level digital control voltage bus, thus giving very coarse step control for the more significant bits (MSBs) and less coarse step control for less significant bits (LSBs). To achieve very fine frequency resolution, the LSB could possibly be operated in analog fashion. A better solution is to dither the LSB digital control bit (or multiple bits) but the problem is that as it occurs in any delta-sigma modulator, the quantization noise is moved to higher frequencies where the phase noise specifications are more challenging. So in designing of the DCO typically considering two or more capacitor banks for fine performance of digital tuning would be useful and to overcome some of the challenges, a delta-sigma modulator, analog filter and considered LC oscillator would have incorporations to reach higher and better performances.

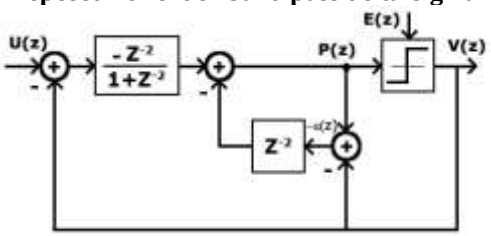
Delta-Sigma Modulator Design:

The main advantage of delta-sigma modulators is that they offer a very good separation of the input signal from the quantization noise due to oversampling and noise shaping. Each delta-sigma modulator is characterized by its order. The first-order delta-sigma modulator is always stable. To avoid the occurrence of instability, it is possible to implement the high-order single-bit delta-sigma modulator by properly cascading first-order stages (Norsworthy, S et al, 1996).

For the quantization error and the signal, the circuit of delta-sigma modulator behaves differently so that the signal would pass unaltered through the modulator, while the quantization noise was high-pass filtered. In this way the quantization noise is separated from the signal in the frequency domain and can be removed by a high precision digital filter (Candy, J. C, 1986).

Figure 4 shows the proposed 4th order band pass delta-sigma modulator. By changing the coupling function of modulator from z^{-1} to $-z^{-2}$, the poles of modulator will displace from $z = 1$ to $z = \pm j$. Based on this conversion, the order of modulator will be twice. But this structure uses coupled noise technique (Lee, K et al, 2007) that decreases the order of loop filter from 2N to N for conversion of non-zero frequency signals. The structure is fully capable to extend into higher order modulators. Using transfer function $-Z^{-4}-2Z^{-2}$ in order to couple the quantization noise to resonator's output, turns the 8th order loop filter to 4th order.

Figure 4: Proposed 4th order band pass delta-sigma modulator



According to Figure 4, the equations for this modulator can be written as follows:

$$e(z) = v(z) - p(z) \tag{3}$$

$$v(z) = \left[(u(z) \quad v(z)) \quad \text{———}\right] + \quad \varepsilon(z) \quad \varepsilon(z) \tag{4}$$

$$v(z) \qquad u(z)z \qquad \varepsilon(z) \times (1 \qquad) \tag{5}$$

(6)

$$(1 \qquad) \tag{7}$$

Proposed Structure:

This paper presents modified DCO architecture that uses a LC-VCO oscillator and 4th order band pass delta-sigma modulator. Employing this combination decreases the phase noise and the distortion of the output signal while the quality of quantization has been improved. By considering an LC tank with high accuracy and proper STF and NTF for the modulator, it could be possible to meet the required criteria. Changing the LC tank's parameters as mentioned above cause to change the frequency of the oscillator. The frequency ***f*** could be controlled by changing either the inductance ***L***, the capacitance ***C***, or some combination thereof. However, in a monolithic implementation, it is more practical to keep the inductor fixed while changing the capacitance of a voltage-controlled device such as a varactor. This LC-VCO structure would become more attractive because of its designing specifications and good fidelity.

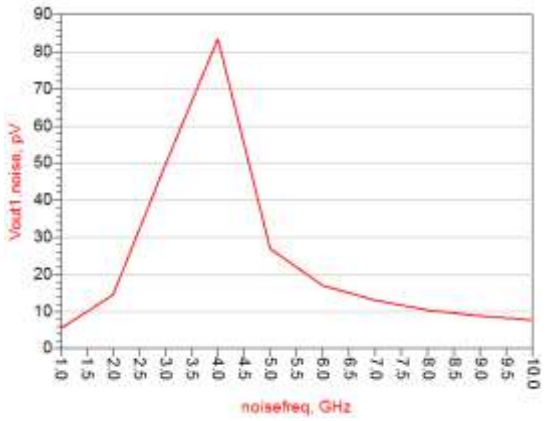
In this study, a band-pass delta-sigma modulator that results from an equivalent low-pass via the transformation $z \rightarrow z^{-2}$ converts a band centered at one fourth of its sampling frequency. The generated pulse sequence is suitable to be used as the clock in discrete-time filters such as the switched-capacitor filters. The problem created by the non-uniform sampling of the analog signal which is caused by the jitter of this clock, is minimized (Bourdopoulos, G et al, 2003). By considering the reduction of quantization noise and phase noise in this structure, it could be visible that the proposed idea improves the circuit output parameters as we need in our application like RF application. In next, the simulation section provides the practical study of this idea.

Simulation Results:

To evaluate the operation of proposed structure, the circuit implemented by using 0.18µm TSMC technology. The main aim of this structure is increasing the quantization's quality in an ADPLL structure by using improved DCO. Obtained results show that in cross-coupled RLC oscillator with oscillation frequency of 3.44GHz, aspect ratio of (W/L=100µm/0.18µm), R=39ohm, C=38.062pF, L=0.05nH present a output noise of 0.6nV,0.55nV and 0.5nV for 1.8GHz, 2GHz and 2.5GHz respectively. In the same way, the proposed LC-VCO with oscillation frequency of 3.84GHz, aspect ratio of (W/L=25µm/0.18µm), L=1nH, C=1pF present a output noise of 13pV, 14pV and 29pV for 1.8GHz, 2GHz and 2.5GHz. But the important point of this result is decreasing the output noise in LC-VCO while the transistor aspect ratio decreased simultaneously. The power consumption of cross-coupled RLC oscillator is 20mW and for proposed LC-VCO is 5.4µW.

When the output noise of oscillator decreased, the operation of quantizing will be improved. As much as the noise decreases the performance of applied structure increases. In Figure 5 the plot of output noise v_s. noise frequency illustrated.

Figure 5: Output noise plotted versus noise frequency



In Figure 6 and Figure 7 the illustration of RLC cross-coupled and LC-VCO output and quantization are depicted. Like the theory of DCO, the simulation of structure shows the advantage of LC-VCO and 4th order band pass delta-sigma modulator combination.

Figure 6: Quantized output of RLC cross-coupled oscillator

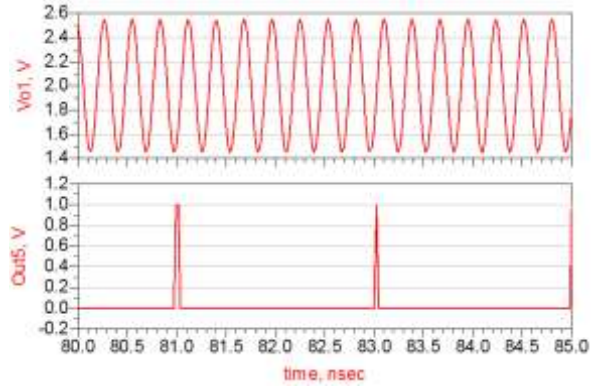
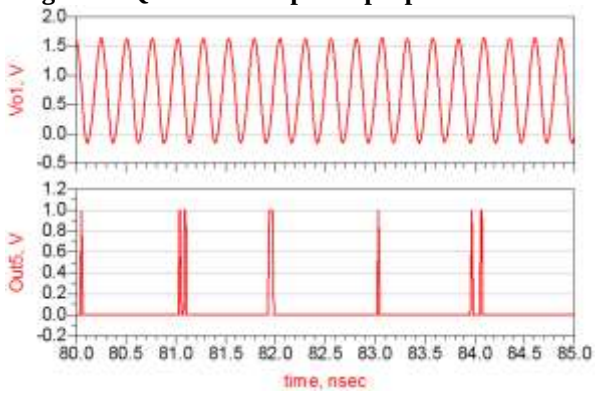


Figure 7: Quantized output of proposed LC-VCO



Conclusion:

The DCO will be improved more in future in line with the advance in CMOS technology for a better performance. DCO has a potential application in RF transceivers, if wide tuning range and small frequency resolution can be attained. The performance, flexibility, and robustness of the proposed DCO suggest that it could be used to construct an entirely digital PLL.

In order to show the improvement in DCO performance a PMOS cross- coupled LC-VCO with low phase noise has been designed and a 4th order band pass delta-sigma modulator attached to it. The proposed structure simulated with TSMC 0.18µm technology to show the result of study. The results confirm that improving the output quantization quality by the modulator which was the result of oscillator good performance and makes this structure favorable in different applications such as RF transceivers. The design of DCO needs to be studied and exploited in the never ending search for faster and high performance DCO implementation.

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