International Academic Institute for Science and Technology

International Academic Journal of Science and Engineering
Vol. 4, No. 2, 2017, pp.210-225.

ISSN 2454-3896

International Academic Journal of Science and Engineering

www.iaiest.com

A Low-Voltage and Low-Power Two-Stage Operational Amplifier Using FinFET Transistors

Vahid Baghi Rahin[a], Amir Baghi Rahin[b]

[a] Department of Electrical Engineering, Sardroud Branch, Islamic Azad University, Sardroud, Iran.

[b] Department of Electrical Engineering, Sardroud Branch, Islamic Azad University, Sardroud, Iran.

Abstract

In this paper, a high gain and low-power FinFET-based amplifier with independent gates is proposed and its design and simulation are performed by HSPICE software and FinFET PTM 32nm technology. The main characteristics of the proposed amplifier such as gain, power consumption, unity gain frequency (UGF), CMRR (common-mode rejection ratio), PSRR (power supply rejection ratio) and settling-time were calculated and compared with a conventional CMOS two-stage amplifier. It was observed that the proposed FinFET-based amplifier has higher performance at lower supply voltage compared to conventional MOSFET-based two-stage amplifier. In the proposed design with the supply voltage of 1 V and 58 µW of power consumption, dc gain of 52 dB and unity gain frequency of 6.4 MHz with a phase margin of 71 degrees were obtained. By comparing the proposed design with conventional CMOS two-stage amplifier in terms of figure of merit it was observed that the figure of merit of the proposed design was improved into 1.2.

Keywords: Two-Stage Operational Amplifier, FinFET Transistor, High Gain, Low-Voltage, Low-Power.

Introduction

Operational Amplifiers (Op-Amps) are one of the main blocks in wide range of analog and mixed-signal systems. Operational amplifiers are used in DC bias to high-speed amplifiers and filters. Speed demand for high speed applications such as ADC and DAC lead to increased demand for amplifiers with high gain and speed. IF switched-capacitor filters and high-precision data converters with high sampling rates

require highly accurate amplifiers with short relaxation times (in the step response). Designing an amplifier with high gain and bandwidth is very hard. According to the required specifications, several structures of operational amplifier are designed. Basically, operational amplifiers are voltage amplifiers which are used to achieve high gain by applying differential inputs. The gain is usually between 50 to 60 dB. Given that new generations of CMOS technology tend to have smaller transistor channel length and low supply voltage value, designing operational amplifiers is a challenge for designers.

By the advances in modelling of semiconductors, miniaturization of transistors and improvements in manufacturing processes with the rapid development of computer design tools, integrated circuit market is growing fast. Today, by reducing transistor channel length to a few tens of nanometers, optimization of analog circuits has become difficult. Due to the intrinsic transconductance of the CMOS devices as well as gain reduction due to the effects of short channel appeared in sub-micron CMOS processes, the designs of gain enhancement have been reported in the literature to increase the gain of operational amplifier (Gray and Meyer, 1974; Johns and Martin, 1996; Huijsing et al., 1995; Allen and Holberg, 2002). These methods of gain enhancement have complex circuit structures and require higher supply voltages and may limit the output voltage swing. Multistage amplifiers may also be used to enhance analog circuits' gain. However multistage amplifiers usually have a compensation problem. Several compensation designs have been introduced and reported in the literature for multistage amplifiers (Gray and Meyer, 1974; Johns and Martin, 1996; Huijsing et al, 1995; Black et al., 1980). Similar techniques in feedback control systems such as lead-lag, pole splitting, nested miller compensation and variable components of signal level have been made for them. However, most methods require a great circuit level and more sophisticated design than the dominant pole approach used in classical operational amplifier.

The reduced MOSFET scale into nanotechnology reveals many challenges such as leakage current, Gate-Induced Drain Leakage (GIDL), the off-state leakage current, delays, power dissipation, short-channel effects and so on. These challenges are inevitable because the transistor size is the most important parameter that should be considered by the designer in the process of size reduction (Suzuki et al., 1994). ITRS institute, in 2006, updated a report in which MOSFET size reduction to 32-nanometer technology production was revealed (Wong, 2001). To overcome the problem of MOSFET size reduction in the field of nanoscale, ITRS introduced an alternative to implementation of such structures as fully depleted SOI with ultra-thin body and multi gate MOSFETs (FinFETs) to the industry. FinFET is a new alternative structure for MOSFET that allows the transistors to be scaled into smaller sizes and has many advantages over MOSFET such as higher drain current, lower switching voltage and 90% reduction in static leakage current (Suzuki et al., 1994). FinFET technology was originally developed by the University of California and its outstanding professors Chenming Hu, Tsu-Jae King-Liu and Jeffrey Bokor (Tosaka, 1994).

As noted above, the tendency to low-power applications requires new structures for operational amplifiers. In control and high precision tools, designing high-gain operational amplifier is necessary. Accordingly, in this article, we are going to introduce a new operational amplifier with high gain and low power consumption using FinFET for better understanding of multi gate devices and present the advantages of the proposed design to increase and improve the main parameters of an amplifier including gain and unity gain frequency. In this article, it has been attempted to cover the studies and research carried out with the FinFET transistor in designing low-voltage and low-power analog integrated circuit to improve operational amplifiers' performance.

FinFET Transistor Review

In 1965, Gordon Moore predicted that the number of transistors per chip will be quadrupled every three years (Colinge, 2008). In order to continue this process, the dimensions of the transistors must be halved every three years. In the 1980s, sub-micron level overcome circuit design and SOI devices were introduced in the 1990s (Colinge, 2008). They offered improved circuit speed and power supply. But, as the transistor dimensions shrink, the close adjacency between the source and drain reduces the ability of gate electrode to control the potential distribution and current flows in the channel. This issue increases electrostatic effect of the source and drain electrodes on the channel. As a result, short-channel effects become prominent. In order to reduce short-channel effects it is necessary to increase gate to channel coupling compared to the source and drain coupling to the channel. But, this leads to an increase in band-to-band tunnelling, Gate-Induced Drain Leakage (GIDL) and greater variability due to the doping level functions of the channel. These limitations can be overcome by double gate MOSFETs (DGFETs). By additional gate, the gate-to-channel coupling is doubled and the short channel effects are stopped (Colinge, 2008; Amara et al., 2009).

The main idea of double-gate MOSFET is that we should have a narrow Si channel and control Si channel by applying the gate contacts to the both sides of the channel. The double-gate concept can be gained by FDSOI structure (Colinge, 2008). If the buried oxide thickness to the gate dielectric is reduced and the ground plate is electrically connected to the transistor's gate, the grounded plate acts as the second gate. The double-gate structure is formed as non-doping channel that is surrounded by the gate electrodes on both sides. The concept of double-gate increases transistors efficiency significantly because their size is reduced compared to planar CMOS. Gate-to-channel coupling is doubled and the short channel effects are easily stopped. Low doping or even non-doping channel can be used in DGFET. This carrier mobility is decreased in size and therefore offers a better intrinsic switching time. Leakage or off-state currents are reduced. DGFET current drive capability, in comparison of planar CMOS, is doubled and so DGFET can work at lower inputs and below the threshold voltages. As a result, power consumption in DGFET is lower. The voltage applied to the gate terminals controls the electric field and determines flow of current through the channel. This provides a sub-threshold slope for the proper performance. So, DGFET can operate at much lower voltages (Colinge, 2008; Amara et al., 2009). DGFET has the following types (Duffy et al.):

1) Planar (horizontal gates and channels).
2) Vertical (direction of conduction is vertical)
3) FinFET (channel is vertical and conduction is parallel to the wafer surface).

FinFET is classified as a multi-gate device. The operating mode of which is most similar to traditional MOSFET. Typically, a source, a drain and a gate are required to control the current. The channel is made between FinFET source and drain that is in the form of a three-dimensional strip on top of silicon substrate (the so-called Fin). With the aim of forming multiple gate electrodes on each side that reduces leakage effects and increases the drive current, the gate is covered around the channel as Figure 1. Also, in previous studies researchers have observed that multi gate devices FinFET have a better immunity against variations which might lead to the self-balance of the two gates (Islam et al., 2011). FinFET devices are produced in different types. In shorted-gate FinFETs (SG-FinFETs), two gates are connected together and lead to the formation of a three-terminal device. It can be used as a direct alternative for traditional bulk-CMOS devices. In independent-gate FinFETs (IG-FinFETs) the upper part of the gate is

delayered and provides two independent gates. Since, the two independent gates can be controlled separately, IG-FinFETs provide more design options (Figure (1)). Four-terminal FinFETs (4T- FinFETs) are widely studies and analyzed in references (Kang and Leblebici, 2003; Agostinelli et al., 2010). Front and back gates of 4T-FinFET can be connected in different structures. One of these structures is to connect both gates with each other. A 4T- FinFET can be considered as two parallel transistors and the two gates can be stimulated independently as shown in Figure 2. One of the gates that normally is called the back gate affects the vertical field of the other transistor in the channel area and changes its threshold voltage. It also affects the diffusion current in the area of subthreshold performance, thus it controls the leakage current. In addition, two parallel transistors in the 4T-FinFET can be connected with each other to improve the driving ability or form a single transistor with independently stimulated gates. This will be helpful in reducing the area and power dissipation in digital circuits (Alioto, 2011). The length and width of device shown in Figure 1 are L_{FIN} and H_{FIN}, respectively (Vinoth et al., 2011). For a greater W_{eff} the design can be performed by several fins aligned in parallel but it is limited to twice the amount of H_{FIN}. Researchers in (Dhulipalla and Lourts Deepak, 2011) have noted that W_{eff} of a FinFET can be expressed as follows:

$$\times (t_{si} + 2H_{FIN}) \tag{1}$$

In the above equation, N_{FIN} is the number of fins in transistor and t_{si} is the fin thickness. Device parameters used in this article are listed in Table 1.

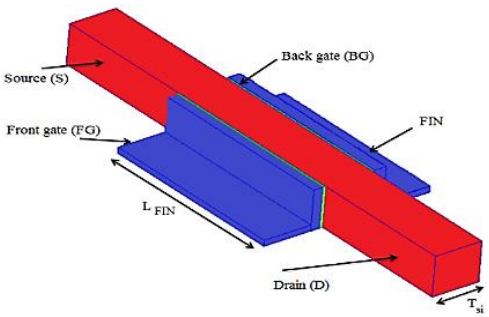


Figure 1: Structure of 4T-FinFET device

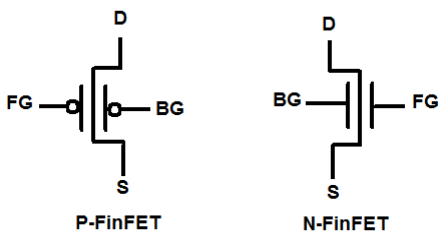


Figure 2: Symbols of n-type and p-type of 4T-FinFET devices

Table 1: Device parameters for FinFET used in this article

Parameter	**Value**
Length of the channel (L)	32nm
Thickness of front/back gate oxide (t_{oxfg}/t_{oxbg})	1.6nm
Thickness of the fin (t_{Si})	8nm
Height of the fin (h_{fin})	32nm
Work function (N/P) (φ_N/φ_P)	4.5eV/4.9eV
Power supply (V_{DD})	1 V
Channel doping (N_{BODY})	2 x 10^{20} cm^{-3}
Source/ Drain doping	2 x 10^{20} cm^{-3}

Proposed Two-Stage Amplifier

FinFET is one of the most promising technologies to design below 50 nm. In order to keep up with technology, transistor sizes must be reduced which leads to several shortcomings in the performance of the transistor. Many of these problems can be solved by FinFET to make better circuit performance. As we attempt to reduce the size, the use of double-gate FinFET transistors in analog circuit design presents significant improvement compared to traditional one gate CMOS design.

Block diagram of an amplifier with a differential input and a single-ended output is shown in Figure 3. According to the block diagram of Figure 3, two-stage amplifier is made of four main components. The components of the two-stage amplifier include: a differential amplifier in the input, second gain circuit, bias circuit and compensation circuit. Given that the circuit load is capacitive, the buffer stage is not required in the amplifier. Differential amplifier at the input obtains a larger share of the total amplifier gain to improve noise performance and offset. To have maximum swing in the output, the second stage is usually used as a simple common source. Compensation circuit is also used to stabilize and the bias circuit has the task of providing the bias voltages of the amplifier circuit. A traditional two stage operational amplifier with compensation capacitor C_c is presented in Figure 4. The amplifier includes the cascode stages of voltage to current (V→I) and current to voltage (I→V) converters (Allen and Hollberg, 2002). The first stage consists of a differential amplifier that converts the differential input voltages to differential currents. The differential currents are applied to the current mirror load that regenerates the differential voltage. This is of course nothing but a differential voltage amplifier. The second stage includes a MOSFET common source that converts the input voltage of the second stage to the current. This op-amp is so much used that is called traditional two stage op-amp. Capacitor C_C is used for Miller compensation to increase the phase margin (Allen and Hollberg, 2002).

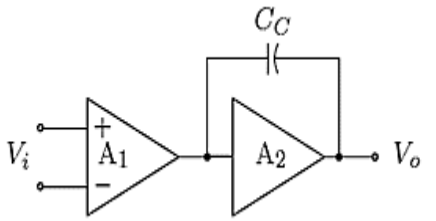


Figure 3: Block diagram of two-stage op-amp

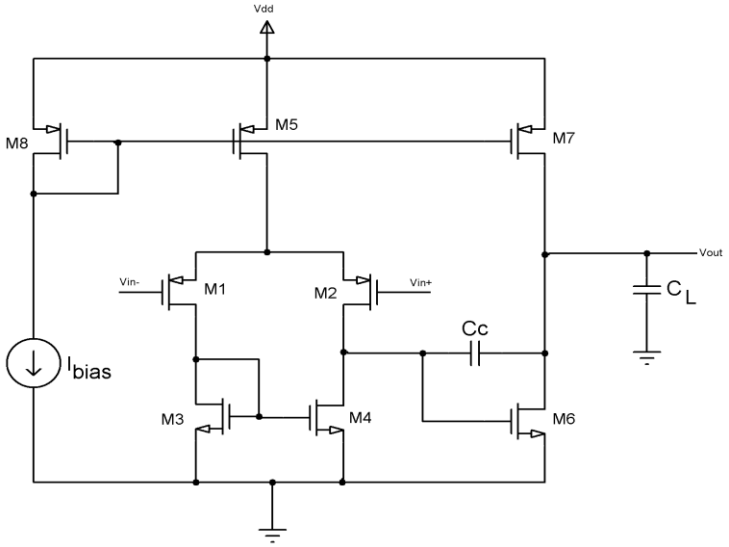


Figure 4: Schematic of two-stage CMOS op-amp with compensation circuit

Here, a new two-stage single-ended differential amplifier with FinFET technology is introduced. The previous circuit implemented with MOSFET is replaced by FinFET transistors. Figure 5 shows the general structure of the amplifier used for designing. All transistors are FinFET and as shown in the figure the second gate of each n-FinFET transistors are connected to GND and the back gate of p-FinFET transistors are connected to Vdd. In Figure 5, M1, M2, M3, M4 and M5 form the first stage of amplifier. M1 and M2 are differential pair and M3 and M4 are used as the load for the differential pair transistors. M6 and M7 together play the role of common source amplifier and form the second stage of amplifier. M5 plays the role of current source to the amplifier. M8 together with I_{bias} plays the role of bias circuit for the amplifier. C_c is used for Miller compensation in the amplifier structure.

Important parameters of an amplifier include open loop gain, unity gain frequency (UGF), slew rate (SR) and settling-time. Here, these parameters in the proposed structure are addressed.

The amplifier open loop gain can be expressed as the multiplication of two stages:

$$\overline{I_6\times(\lambda_2+\lambda_3)\times(\lambda_6+\lambda_7)} \quad (2)$$

Therefore, the gain depends to transconductance g_m and the channel length modulation parameter λ. FinFET effective mobility is higher than bulk transistors due to non-doping channels and as a result

increases g_m (Yu et al., 2001). Channel length modulation parameter (λ) in FinFET is considerably minimized due to better control of short channel effects in double-gate structure. So, the gain can be increased by FinFET.

The ratio of change in output voltage caused by a step input is called slew rate (SR). Its value depends on the amount of compensation capacitor C_c and the current I_5 that can be mentioned as follows (Wong, 2001):

— (3)

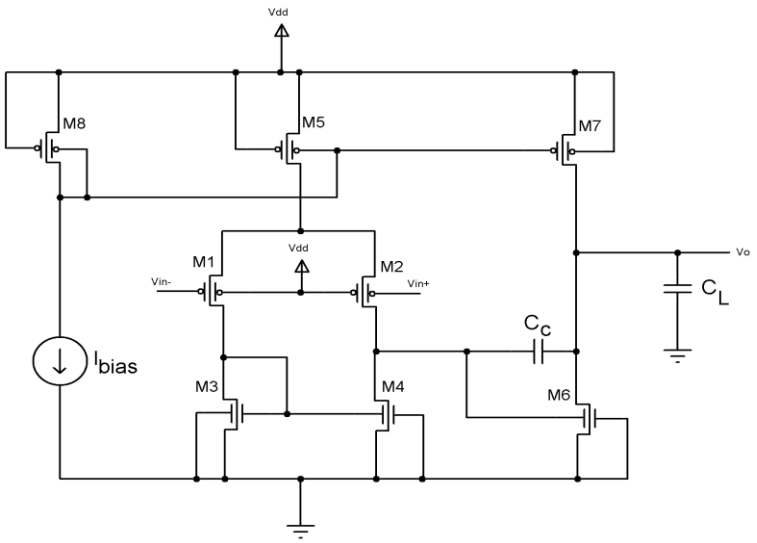


Figure 5: Schematic of proposed two-stage FinFET op-amp with compensation circuit

Now, the transconductance g_m in the proposed structure is more than single-gate MOSFET and leads to a good phase margin for the proposed uncompensated operational amplifier. Thus, a smaller amount of C_C is necessary for FinFET operational amplifier. Also, the drive current of FinFET is twice greater than traditional bulk MOSET. So, I_5 for FinFET structure is higher and the slew rate is greater.

Unity gain frequency (UGF) determines the frequency at which the gain voltage is unit. UGF is expressed as follows:

— (4)

As discussed above, g_m is greater for the FinFET operational amplifier and C_C amount is lower. So, unity gain frequency is larger and thus gain-bandwidth product increases.

When the output of operational amplifier is entered to a certain amount of final amount it is called settling-time (t_s). Basically, its value depends on the bandwidth and the SR (Suzuki et al., 1994) and both of these values are large in the FinFET operational amplifier. In addition, FinFET has a faster switching time than the single gate MOSFET. Therefore, settling-time for FinFET operational amplifier is larger.

Simulation Results

The conventional two-stage amplifier was designed in PTM 32nm CMOS process and proposed double-gate amplifier was designed in PTM 32nm FinFET process and simulated by HSPICE software. Analyses of DC, AC, output swing, CMRR, PSRR and settling-time were performed and output figures are shown as follows.

Frequency response of conventional two-stage CMOS amplifier and proposed two-stage FinFET amplifier for different supply voltages are presented in Figures 6 and 7, respectively. In these figures, the output voltage gain and output voltage phase charts are plotted logarithmically.

CMRR frequency response of conventional two-stage CMOS amplifier and proposed two-stage FinFET amplifier for different supply voltages are presented in Figures 8 and 9, respectively. CMRR value of the conventional two-stage CMOS amplifier for voltages ranging from 1 to 0.4 volts is 53, 50.3, 45.4, 38, 31, 25.1 and 20.9 dB. Also, CMRR value of the proposed two-stage FinFET amplifier for voltages ranging from 1 to 0.4 volts is 47.9, 47.6, 49.1, 48.2, 46.6, 41.3 and 30.4 dB.

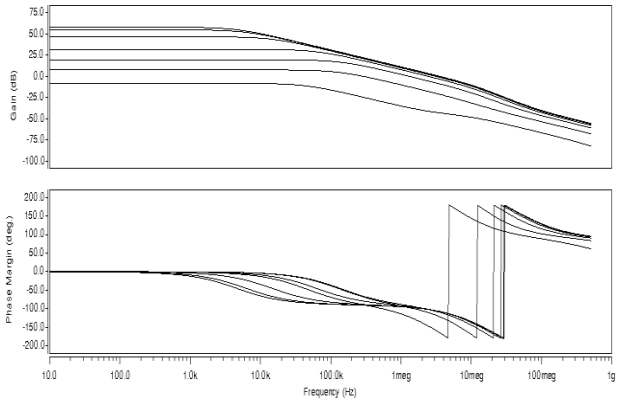


Figure 6: Bode plot of conventional two-stage CMOS amplifier for various supply voltage

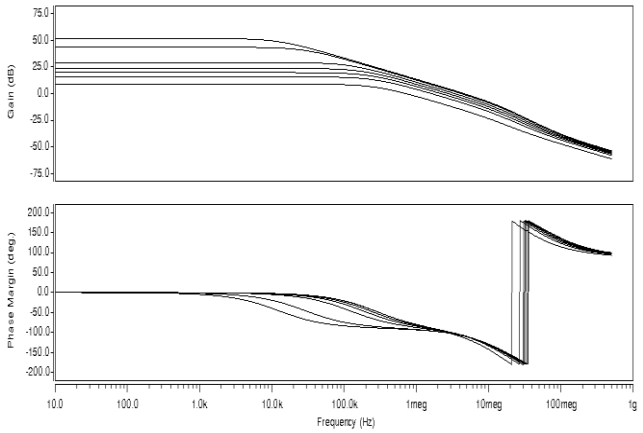


Figure 7: Bode plot of proposed two-stage FinFET amplifier for various supply voltage

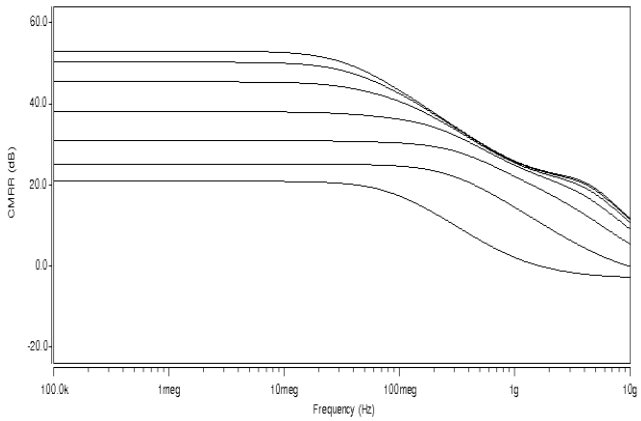


Figure 8: CMRR of conventional two-stage CMOS amplifier for various supply voltage

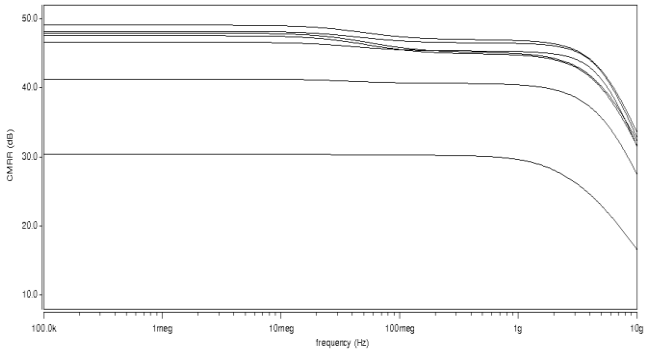


Figure 9: CMRR of proposed two-stage FinFET amplifier for various supply voltage

The output voltage swing of conventional and proposed two-stage amplifier for a supply voltage of 1 V are presented in Figs. 10 and 11, respectively. Obviously the conventional amplifier output swings within the range 125 mV to 885 mV and it is possible to have 0.76 V swing in the output. It is clear from Figure 11 that the output of the proposed amplifier swings in the range of 100 mV to 900 mV thus it is possible to have 0.8 V swing in the output.

PSRR is the ability of an amplifier to eliminate the ripple noise from the supply line which is discussed as figure of merit. PSRR+ frequency response of conventional two-stage CMOS amplifier and proposed two-stage FinFET amplifier for different supply voltages are presented in Figures 12 and 13, respectively. PSRR+ value of the conventional two-stage CMOS amplifier for various supply voltages is 54.9, 48.1, 39, 28.5, 17.7, 15.2 and 13.7 dB. Also, PSRR+ value of the proposed two-stage FinFET amplifier for various supply voltages is 42.5, 42.3, 42.3, 40.4, 36.9, 29.7 and 16.5 dB.

PSRR- frequency response of conventional two-stage CMOS amplifier and proposed two-stage FinFET amplifier for different supply voltages are presented in Figures 14 and 15, respectively. PSRR- value of the conventional two-stage CMOS amplifier for various supply voltages is 32.1, 29.6, 26, 20.2, 11.9, 2.48 and -1.03 dB. Also, PSRR- value of the proposed two-stage FinFET amplifier for various supply voltages is 32.4, 32.3, 31.8, 30.2, 26.8, 21.3 and 11.6 dB.

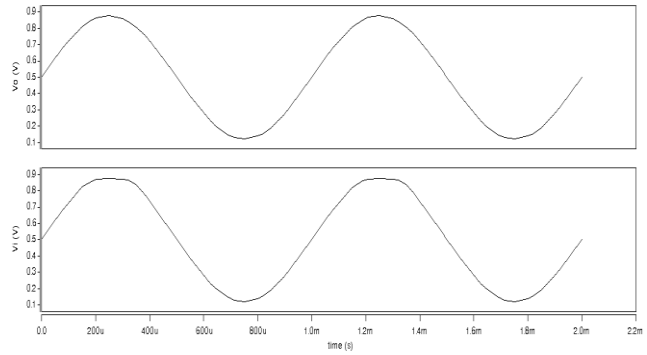


Figure 10: Output voltage swing of conventional two-stage CMOS amplifier

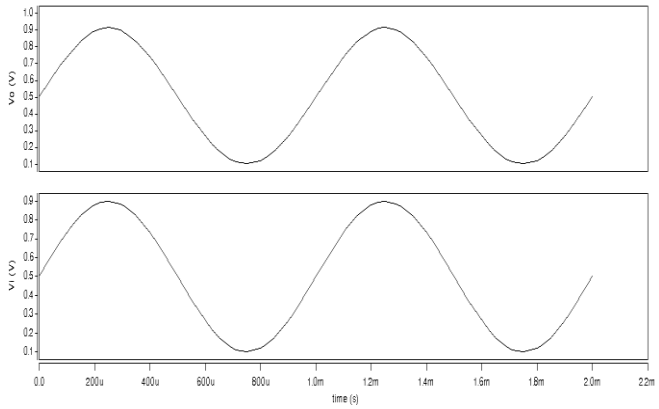


Figure 11: Output voltage swing of proposed two-stage FinFET amplifier

For different supply voltages, settling-time of the conventional and proposed two-stage amplifier are presented in Figures 16 and 17, respectively. Settling-time of the conventional two-stage CMOS amplifier for various supply voltages are equal with 0.33, 0.38, 0.39, 1, 2 and 5 µs. Figure 17 indicates that up to the supply voltage of 0.5V, settling-time of the proposed amplifier is 0.35 µs and in the supply voltage of 0.4V, settling-time of the proposed amplifier approaches 1 µs.

In Figure 18, a summary of the conventional and proposed two-stage amplifier simulation results are shown on the charts by varying the supply voltage for better evaluation. In this figure, the charts of the power consumption, dc gain, unity gain frequency, CMRR, PSRR and settling-time are presented. It is clearly observed that using FinFET with two independent gates increases two-stage operational amplifier performance considerably.

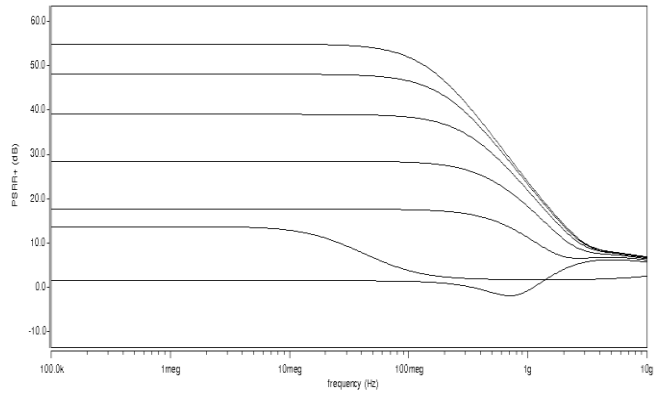


Figure 12: PSRR+ of conventional two-stage CMOS amplifier for various supply voltages

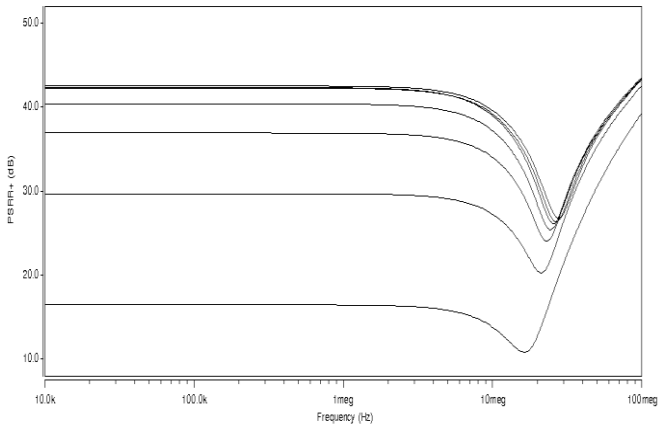


Figure 13: PSRR+ of proposed two-stage FinFET amplifier for various supply voltages

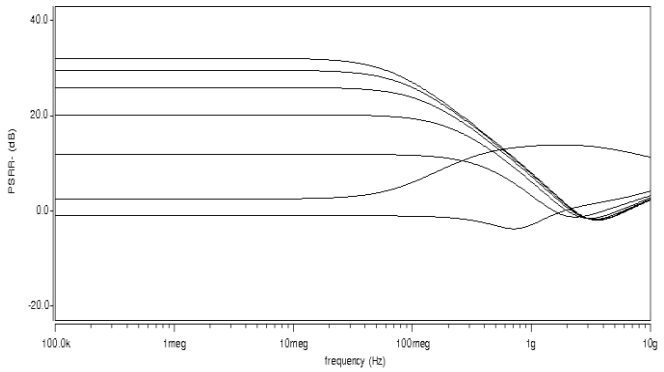


Figure 14: PSRR- of conventional two-stage CMOS amplifier for various supply voltages

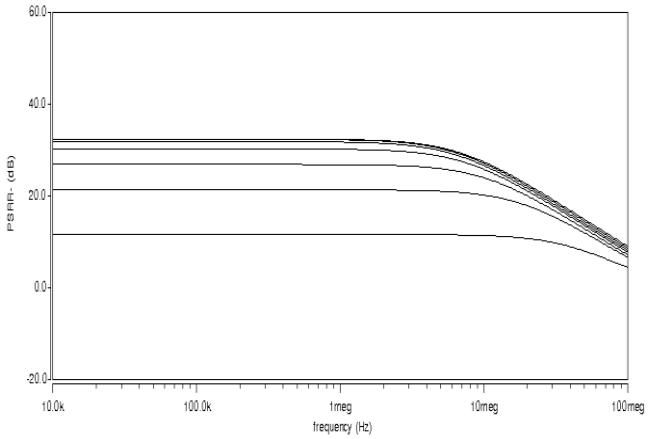


Figure 15: PSRR- of proposed two-stage FinFET amplifier for various supply voltages

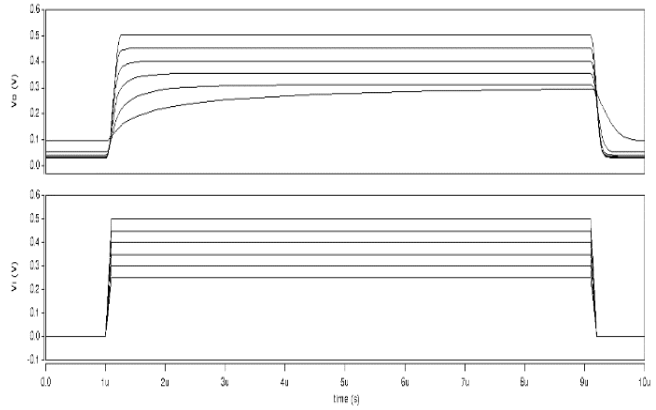


Figure 16: Settling-time of conventional two-stage CMOS amplifier for various supply voltages

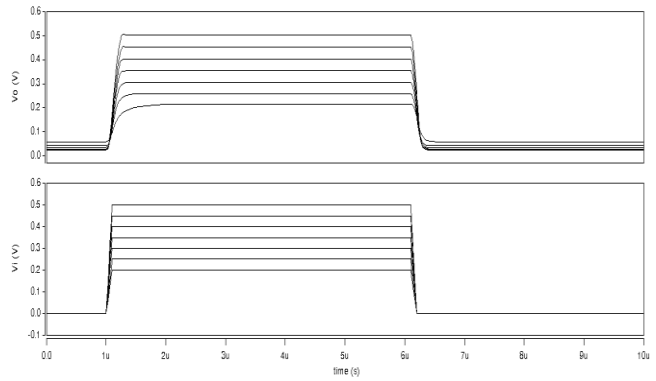
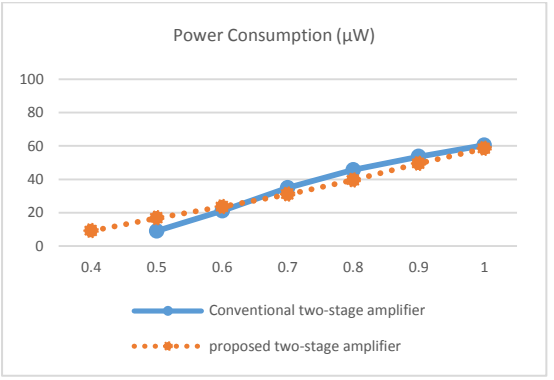
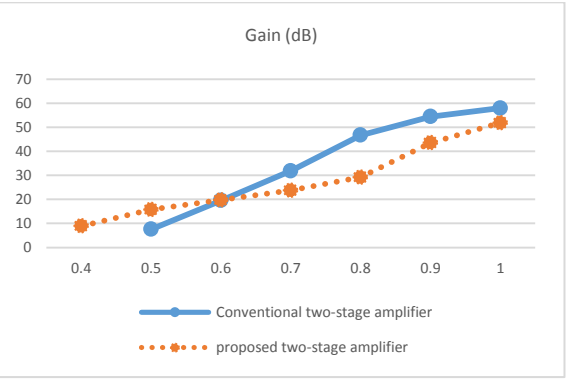


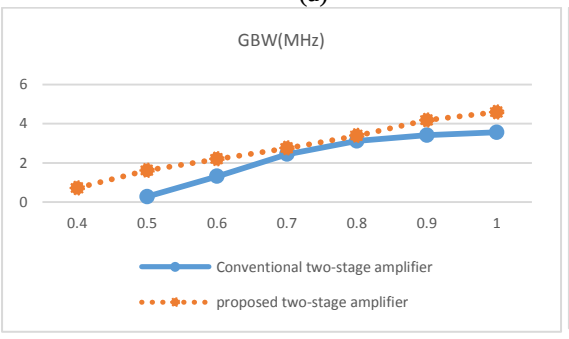
Figure 17: Settling-time of proposed two-stage FinFET amplifier for various supply voltages


Power Consumption (μW)
100
80
60
40
20
0
0.4
0.5
0.6
0.7
0.8
0.9
1
Conventional two-stage amplifier
proposed two-stage amplifier

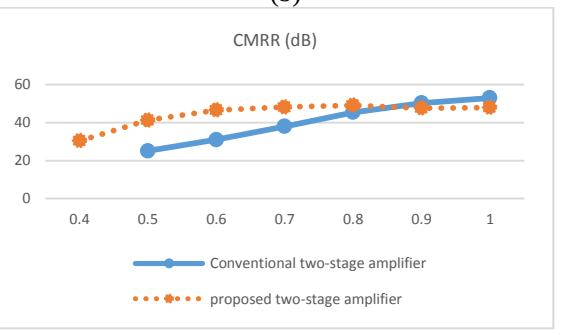
(a)


Gain (dB)
70
60
50
40
30
20
10
0
0.4
0.5
0.6
0.7
0.8
0.9
1
Conventional two-stage amplifier
proposed two-stage amplifier

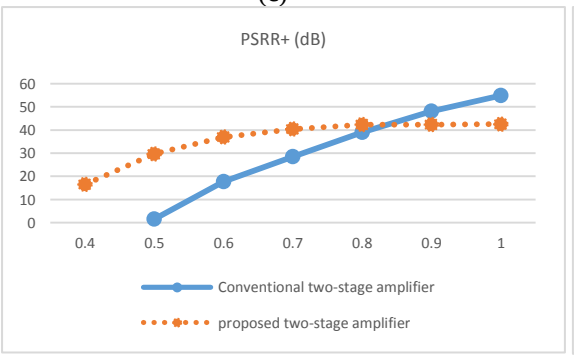
(b)


GBW(MHz)
6
4
2
0
0.4
0.5
0.6
0.7
0.8
0.9
1
Conventional two-stage amplifier
proposed two-stage amplifier

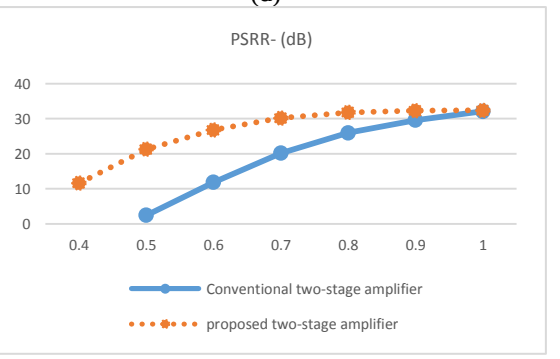
(c)


CMRR (dB)
60
40
20
0
0.4
0.5
0.6
0.7
0.8
0.9
1
Conventional two-stage amplifier
proposed two-stage amplifier

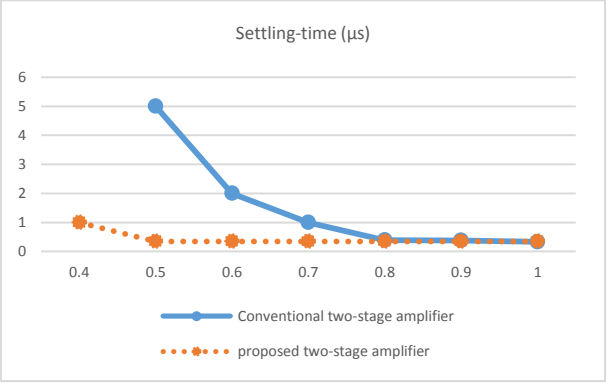
(d)


PSRR+ (dB)
60
50
40
30
20
10
0
0.4
0.5
0.6
0.7
0.8
0.9
1
Conventional two-stage amplifier
proposed two-stage amplifier

(e)


PSRR- (dB)
40
30
20
10
0
0.4
0.5
0.6
0.7
0.8
0.9
1
Conventional two-stage amplifier
proposed two-stage amplifier

(f)



(g)

Figure 16: Response of conventional and proposed two-stage amplifier for various supply voltage: (a) power consumption, (b) dc gain, (c) unity gain frequency, (d) CMRR, (f) PSRR+, (f) PSRR- and (g) settling-time

By comparing the proposed two-stage amplifier with the supply voltage of V_{dd}=0.5V and conventional two-stage amplifier with the supply V_{dd} =0.5V, it can be observed that the proposed amplifier with an increase of two times in the power consumption presents higher voltage gain. Other parameters such as SR, UGF and settling-time for the proposed amplifier are greater than the conventional structure using MOSFET. Therefore it can be concluded that the proposed amplifier using FinFET can be used in low voltage and low power applications and has a good performance compared to the MOSFET based structures.

For a more detailed assessment of the proposed amplifier a figure of merit (FoM) is suggested as ———— . The figure of merit of the proposed amplifier is shown in Figure 18 and the proper amplifier performance using FinFET is determined.

Conclusion

In this paper, using FinFET was investigated in the two-stage amplifier structure. Accordingly, the conventional two-stage amplifier in 32nm CMOS process and the proposed amplifier in 32nm FinFET process and double-gate transistors with independent gate were designed and simulated by the supply voltage of 1 V. Variations in the supply voltage on the performance of both structures were studies for different voltages between 1 and 0.4 V. In both simulated amplifiers the capacitance load was considered as 10 pF and the value of the compensation capacitor in both designs was 2.2 pF. Most important parameters of an operational amplifier were evaluated. According to the results, the proposed amplifier presented a good performance up to the supply voltage of 0.4V but the conventional amplifier had a good performance up to the supply voltage of 0.5 V.

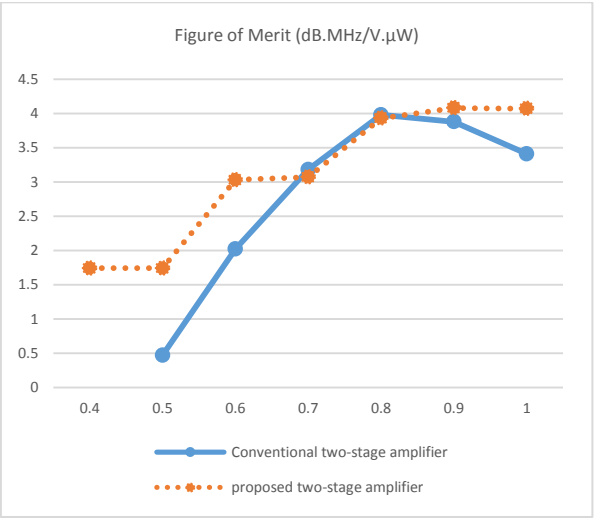


Figure 18: Figure of merit for conventional and proposed two-stage amplifier with supply voltage variation

References

Agostinelli, M., Alioto, M., Esseni, D., & Selmi, L. (2010). Leakage delay tradeoff in finfet logic circuits: a comparative analysis with bulk technology. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, vol. 18, no. 2, pp. 232–245.

Alioto, M. (2011). Comparative evaluation of layout density in 3T, 4T, and MT FinFET standard cells. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, vol. 19, no. 5, pp. 751–762.

Allen, P.E., & Holberg, D.R. (2002). CMOS Analog Circuit Design. 2nd Ed. New York: Oxford University Press.

Amara, A., Rozeau O., & Editors. (2009). Planar Double-Gate Transistor: From Technology to Circuit. Springer, pp. 1-20.

Black, W., Allstot, D., & Reed, R. (1980). A high performance low power CMOS channel filter. IEEE J. Solid-State Circuits, vol. SC-15, no. 6, pp. 929–938.

Colinge, JP., & Editors. (2008). FinFET and Other Multi-Gate Transistors. Springer, 2008, pp 1-13.

Dhulipalla, L., & Lourts Deepak A. (2011). Design and implementation Of 4-bit ALU using FINFETS for nano scale technology," Nanoscience, Engineering and Technology (ICONSET), 2011 International Conference on, pp. 190-195.

Duffy, M., Dattoli, E., & Espinosa, A. Nanoscale Silicon Technology. http://www.guo.ece.ufl.edu/project4.ppt.

Gray, P., & Meyer, R. (1994). Recent advances in monolithic operational amplifier design. IEEE Transactions on Circuits and Systems, vol. CAS-21, no. 3, pp. 317–327.

Huijsing, J., R. Hogervorst, & de Langen, K.-J. (1995). Low-power low-voltage vlsi operational amplifier cells. IEEE Transactions on Circuits and Systems, vol. 42, no. 11, pp. 841–852.

Islam, A., Akram, M., & Hasan, M. (2011). Variability Immune FinFET-Based Full Adder Design in Subthreshold Region. Devices and Communications (ICDeCom), IEEE International Conference, pp. 1-5.

Johns, D., & Martin, K. (1995). Analog Integrated Circuit Design. New York: John Wiley & Sons, Inc.

Kang, S. M., & Leblebici Y. (2003). CMOS Digital Integrated Circuits Analysis and Design. McGraw-Hill, New York, NY, USA.

Suzuki, K., Tanaka, T., Tosaka, Y., Horie, H., Arimoto, Y., & Itoh T. (1994). Analytical surface potential expression for thin-film double-gate SOI MOSFETs. Solid-State Electronics, vol.37, no. 2, pp. 327–332.

Suzuki, K., & Sugii T. (1995). Analytical models for n+-p+ double-gate SOIMOSFET's. IEEE Transactions on Electron Devices, vol.42, no. 11, pp. 1940–1948.

Tosaka, Y., Suzuki, K., Horie, H., & Sugii, T. (1994). Scaling-parameter-dependent model for subthreshold swing S in double-gate SOI MOSFET's. IEEE Electron Device Letters, vol.15, no.11, pp.466–468.

Vinoth, C., Bhaaskaran, V. S. K., Brindha, B. & et al. (2011). A novel low power and high speed Wallace tree multiplier for RISC processor. in Proceedings of the 3rd International Conference on Electronics Computer Technology (ICECT '11), pp. 330–334.

Wong, H. S. P. (2001). Beyond the conventional MOSFET. in Proceeding of the 31st European Solid-State Device Research Conference, pp.69–72.

Yu, B., Wang, H., Joshi, A., Xiang, Q., Ibok, E., & Lin, M. (2001). 15 nm gate length planar CMOS transistor. in Proceedings of the International Electron Devices Meeting. Technical Digest (IEDM '01), pp. 937–939.